OPERATING VOLTAGE CONSTRAINTS AND DYNAMIC RANGE IN ADVANCED SILICON-GERMANIUM HBTS FOR HIGH-FREQUENCY TRANSCEIVERS

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OPERATING VOLTAGE CONSTRAINTS AND DYNAMIC RANGE IN ADVANCED SILICON-GERMANIUM HBTS FOR HIGH-FREQUENCY TRANSCEIVERS

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SUMMARY

Based on its performance capabilities, low cost, and capacity for high-integration, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) BiCMOS technology has established itself as strong technology contender for a host of circuit applications including analog, mixed-signal, RF and millimeter-wave. However, as operating frequencies for wireless applications are pushed upward in the spectrum, SiGe HBT technologies face significant challenges at the transistor-level as operating voltage limits decrease and performance requirements increase. This work will investigate operational voltage constraints and dynamic range for state-of-the-art SiGe HBTs.

The fundamental limits related to avalanche breakdown and linearity performance of SiGe HBTs will be comprehensively examined at the transistor-level across multiple technology generations, and the corresponding circuit-level impacts for high-frequency transceiver blocks will be evaluated. The bias dependencies of avalanche breakdown instabilities will be analyzed, and performance and reliability of SiGe HBTs under aggressive bias conditions will be studied. Breakdown instabilities will also be investigated in the context of extreme environments. Linearity will be studied across bias and geometry at the transistor-level to understand the limits and trade-offs of achieving high dynamic range performance in SiGe HBTs. Simple expressions for common-base linearity will be derived from analysis of the SiGe HBT using Volterra series. Based on these studies, circuit-level design techniques for robust performance and enhanced dynamic range will be proposed, and new RF circuit designs using these techniques will be presented.

The following items summarize new contributions to the field made by this work.

1. The first-ever comprehensive analysis of the effects of scaling and bias on operating voltage constraints in advanced SiGe HBTs [20].

2. Novel analysis of factors contributing to common-base avalanche instabilities in SiGe HBTs [21].

3. An investigation of operating voltage constraints for SiGe HBTs operating in extreme environments [22], [23].

4. Analysis of large-signal RF performance, linearity, and reliability of SiGe HBTs under aggressive bias conditions [24].

5. Novel investigation of large-signal RF operating limits for SiGe HBTs, with new expressions describing the RF safe-operating area [25].

6. Investigation of common-base intermodulation distortion with new expressions for linearity performance derived from Volterra series analysis [26].

7. Novel circuit designs, including an aggressive-cascode power amplifier for improved power density, and a low-noise amplifier with enhanced dynamic range performance [27].

CHAPTER I

INTRODUCTION

1.1 Motivation

1.1.1 Role of SiGe HBTs in Emerging Wireless Applications

Next-generation wireless systems, driven by a vast assortment of rapidly-emerging applications operating at RF and millimeter-wave (mmW) frequencies, will place increasingly stringent cost and performance demands upon the supporting microelectronics technologies. These emerging systems encompass a variety of areas in both the government and consumer sectors, including communications, radar, and imaging applications. The operating frequencies for these applications is determined by a variety of factors ranging from government regulation and allocations of spectrum to natural phenomena such as environmentally-dependent attenuation bands across frequency. But in general, a push to higher operating frequencies is motivated by several benefits, including:

1. Greater spectrum availability at higher frequencies compared to lower frequency bands, which are often crowded with existing users.

2. Larger proportional bandwidth at higher frequency, which allows for fewer constraints on signal modulation and increased frequency agility.

3. Shorter wavelengths, which allow for smaller antenna sizes and translates to smaller, more portable systems.

4. Narrow radiated beams for high angular resolution for greater directivity, which results in lower interference and higher security transmissions.

With steady performance gains and continued innovation in process integration, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) BiCMOS technology is becoming an increasingly viable and affordable solution for highly integrated, high-performance mixed-signal applications [1]. Because of careful bandgap engineering, lateral scaling, and vertical profile optimization, state-of-the-art SiGe HBTs currently demonstrate peak unity-gain cutoff frequency (f_T) in excess of 350

GHz [2]. This level of performance far exceeds that of standard Si BJTs and rivals the best III-V technologies, yet comes with the yield and cost advantages associated with Si fabrication. The compatibility of SiGe HBTs with Si permits higher yield and superior levels of system complexity and integration, leveraging the benefits of best-of-breed Si CMOS to offer powerful "mixed-signal" solutions. With the ability to fabricate high-performance analog and RF circuits alongside powerful CMOS logic on a single silicon wafer, SiGe HBT BiCMOS technology enables powerful system-on-a-chip (SoC) architectures that facilitate reduced chip count, lower power consumption, reduced packaging complexity, and overall lower cost [1].

The benefits offered by SiGe HBT mixed-signal ICs make this technology an attractive alternative for a host of emerging wireless applications at higher frequency bands. Of particular interest are transceivers operating above 10 GHz for a wide range of RF and millimeter-wave (mmW) applications in both the government and consumer sectors. Examples include X-band phased-array radar systems for missile defense (8.5–12.5 GHz), wideband electronic warfare (EW) and electronic support measures (ESM) systems (2–20 GHz), satellite communications systems (14 and 20+ GHz), automotive radar (24 and 94 GHz), and secure point-to-point high bandwidth wireless local-area-networks (WLANs). However, as operating frequencies for wireless applications are pushed upward in the spectrum, SiGe HBT technologies face significant challenges at the transistor-level in terms of supporting systems that achieve adequate propagation distance (transmitter output power, or receiver input sensitivity), acceptable signal quality (dynamic range), and reliable operation (safe-operating area). Therefore, the development of affordable, highly integrated next-generation wireless communications systems based on SiGe HBT BiCMOS technologies requires the study and understanding of these limitations at their fundamental device level.

In addition to transistor performance and reliability, the distortion characteristics and dynamic range of SiGe HBTs must be carefully considered. The term dynamic range (DR) refers to the ratio between the maximum and minimum input signal levels for which a circuit or system can provide acceptable signal quality. At its lower bound, the dynamic range for an RF block is defined by the minimum detectable signal (MDS), which is determined by the noise threshold of the block and signal-to-noise ratio (SNR) requirements of the system. The upper limit of the dynamic range is determined by the distortion characteristics (nonlinearities) of the block. Achieving high DR poses

a critical issue for modern transceivers. For the purposes of this work, distortion is generally categorized into one of two domains: intermodulation distortion, which occurs for small-signal operation and primarily affects receiver (RX) dynamic range, and large-signal distortion such as such as RF gain compression, which primarily affects transmitter (TX) dynamic range and is strongly influenced by *dc* operating conditions and the limits of the dynamic output current and voltage swing.

1.1.2 Operating Voltage Limits

Operating voltage limits, as dictated by avalanche breakdown effects, represent a significant challenge to transistor reliability, performance, and large-signal dynamic range, particularly as transistors are scaled to operate at higher frequencies. Achieving higher frequency performance (increased peak f_T) in SiGe HBTs typically requires operation at higher current densities. This trend is shown in Figure 1 for three generations of SiGe HBT BiCMOS technology. To operate at higher current density requires increased collector doping to suppress the Kirk effect and heterojunction barrier effects. This leads to an increase in the impact-ionization rate at the collector-base junction [3] and results in the well-known trade-off between peak f_T and breakdown voltage (BV) inherent to SiGe HBT device design [4]. This trend is depicted in Figure 2 for various breakdown voltage (BV) parameters, including open-base breakdown (BV_{CEO}), open-emitter breakdown (BV_{CBO}), and the critical collector voltage ($V_{CB-crit} + V_{BE}$) for common-base operation at fixed I_E drive (CB-I_E).

This trade-off between BV and f_T poses important design challenges for transceivers operating at higher frequencies, particularly with regards to achieving adequate RF power on the transmit side. Consider a transistor used in a typical Class A power amplifier (PA). The maximum output power is roughly proportional to (assuming negligible knee voltage V_{Knee}) the product of the maximum voltage (V_{MAX}) and maximum current (I_{MAX}) of the load-line characteristics (see Figure 3), and can be written as

$$P_{out} = \frac{(V_{MAX} - V_{knee}) \cdot I_{MAX}}{8}. \tag{1}$$

The maximum voltage is dictated by the ever-decreasing BV of the transistor.

Besides output power, another key consideration for RF transmitters is power-added efficiency (PAE), which is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}, \tag{2}$$

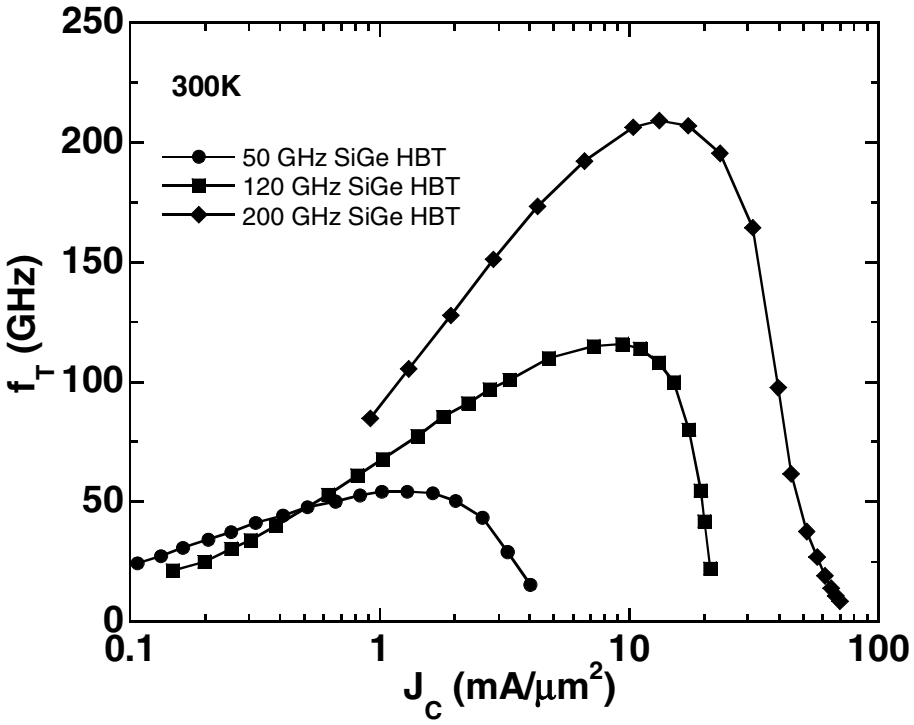

Figure 1: Cutoff frequency (f_T) as a function of collector current density for three generations of SiGe HBT BiCMOS technology.

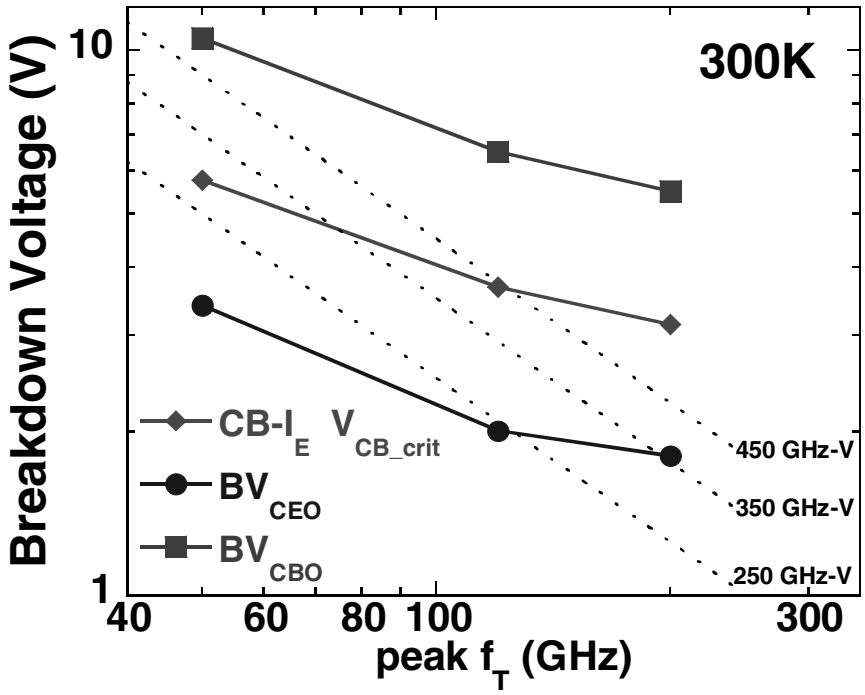

Figure 2: Peak f_T versus BV for three generations of SiGe HBT technology. Contours of constant BV-f_T products (dotted lines) are indicated.

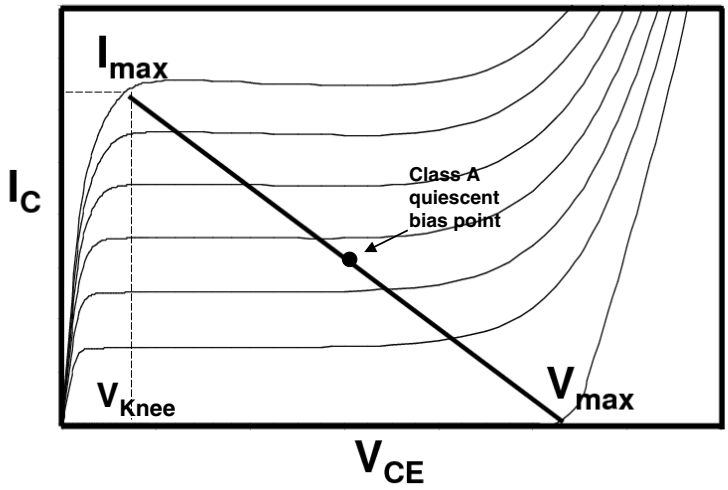

Figure 3: Example load-line transposed over the output characteristics of a typical SiGe HBT.

where P_{in} is the input power and P_{dc} is the dissipated dc power. P_{dc} can be approximated as the product of the quiescent voltage and current at the output, which for Class A operation are $(V_{MAX} + V_{knee})/2$ and $I_{MAX}/2$, respectively. Therefore, given the power gain ($G = P_{out}/P_{in}$), Class A PAE can be rewritten as

$$PAE \approx \frac{1}{2} \cdot \frac{V_{MAX} - V_{Knee}}{V_{MAX} + V_{Knee}} \cdot (1 - 1/G), \tag{3}$$

In the ideal case ($V_{Knee} = 0$ and $G = \infty$), this reduces to 1/2 (50%). These expressions indicate that both P_{out} and PAE suffer as the difference between V_{MAX} and V_{knee} decreases. Moreover, power gain must remain sufficiently high; otherwise PAE will be significantly reduced.

Thus, the decreasing BV in aggressively scaled SiGe HBTs has important implications for high-frequency large-signal performance in terms of the 1-dB compression point (P1dB), saturated power (P_{sat}), and PAE. These challenges at high frequencies are demonstrated in Figure 4, which shows output power as a function of operating frequency reported in the literature for PAs designed using CMOS, SiGe HBT, and InGaP HBT technologies [5]-[12]. Clearly, obtaining adequate output power becomes more difficult for higher-frequency applications. Moreover, the power gain achievable in a single-stage amplifier tends to decrease for higher operating frequencies, as shown in Figure 5, resulting in lower PAE. However, careful choice in circuit architecture, such as the differential cascode approach used in [11], can be leveraged to significantly improve the gain, output power, and PAE compared to standard PA architectures.

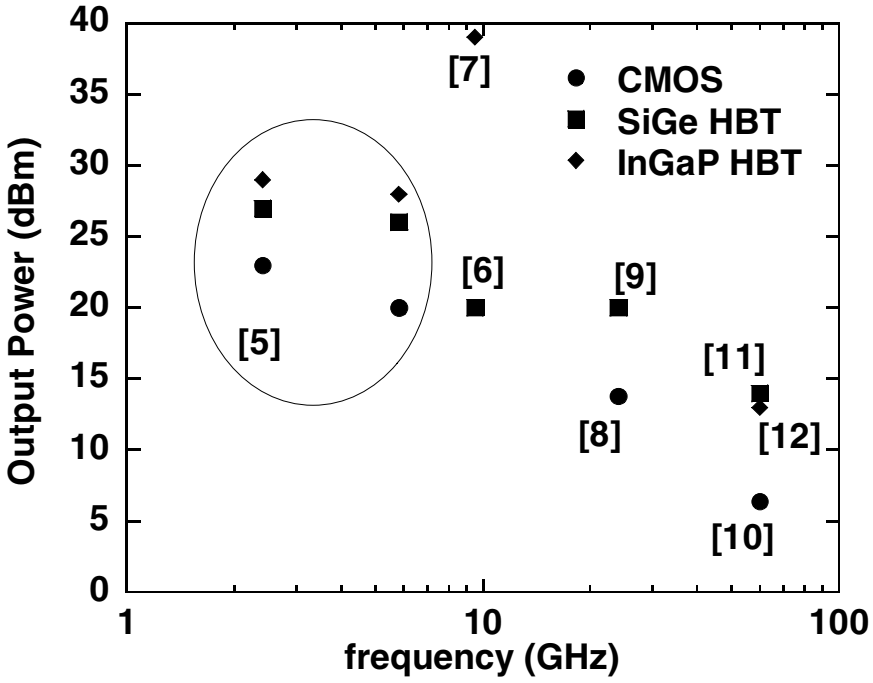

Figure 4: Output power versus operating frequency reported for power amplifiers fabricated using CMOS, SiGe HBTs, and InGaP HBTs.

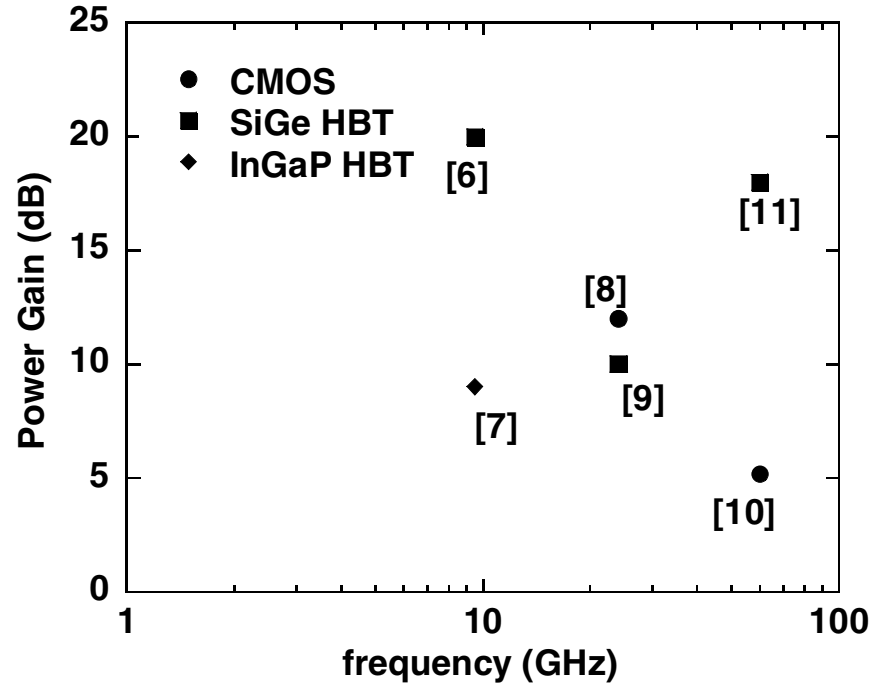

Figure 5: Single-stage power gain versus operating frequency reported for power amplifiers fabricated using CMOS, SiGe HBTs, and InGaP HBTs.

As SiGe HBT BiCMOS technologies scale for higher-frequency performance, circuit designers striving to maintain adequate output power and gain performance must pay careful attention to the complex and increasingly rigorous upper-voltage limits for reliable device biasing and dynamic operation – the so-called "safe-operating area" (SOA) [2]. The ever-decreasing operating voltage limits of scaled SiGe HBTs often pose non-obvious constraints on the biasing and operation of SiGe HBTs used in mixed-signal circuits [13]. Moreover, nonlinearities caused by avalanche multiplication at high collector voltage can contribute to intermodulation distortion, another vital consideration in high-frequency transceivers.

1.1.3 Intermodulation Distortion

Intermodulation distortion (IMD) represents an important consideration in transceiver linearity and dynamic range. IMD for a transistor or circuit is often characterized by a two-tone test, which measures the intermodulation products resulting from two closely spaced in-band signals (f_1 and f_2) at the input. When presented to a nonlinear block, the resulting output spectrum includes various orders of mixing products of the two tones. The mixing products for third-order intermodulation (IM3) are of particular interest because they occur at the output frequencies $2f_1 - f_2$ and $2f_2 - f_1$, and therefore tend to fall within the operating frequency band and are processed alongside the desired signal. Thus, these nonlinearities directly effect receiver sensitivity and degrade signal integrity by contributing to higher bit-error-rate (BER) in digital transmissions and audible or visible defects in analog transmissions.

Both the fundamental output power (P_{out}) and the output intermodulation power (P_{o-IM3}) depend on RF input power (P_{in}) as shown in Figure 6. Under small-signal operating conditions (e.g. backed off considerably from P1dB) P_{out} and P_{o-IM3} have well-defined 1:1 and 3:1 (respectively) relationships with P_{in}, allowing for the reliable extraction of the third-order intercept point (IP3). Because IP3 is independent of P_{in} it serves as a standard figure-of-merit for linearity. The input-referred third-order intercept (in dBm) is

$$\text{IIP3} = P_{in} + \frac{P_{out} - P_{o-IM3}}{2}, \tag{4}$$

with higher IP3 representing lower distortion and better linearity in the amplifier block.

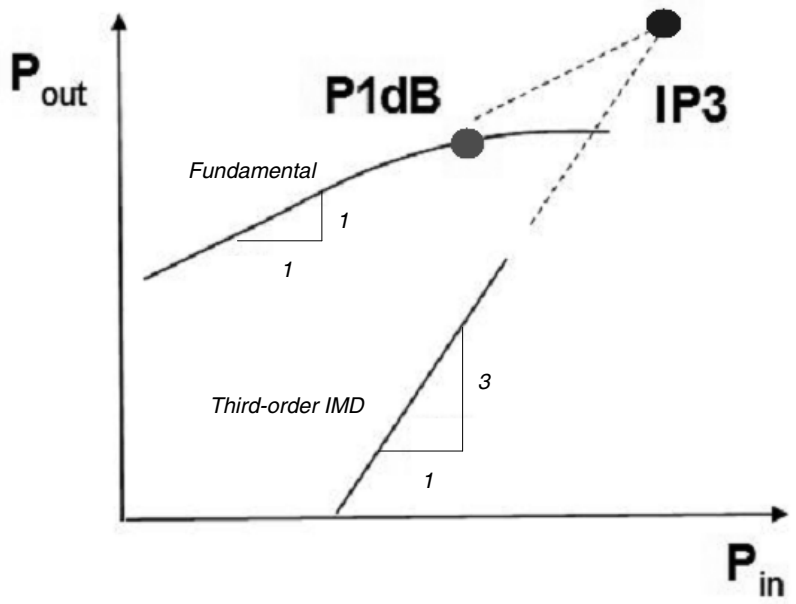

Figure 6: Typical transistor RF power sweep showing the output power of the fundamental and third-order IMD products.

For cascaded gain stages, maintaining high linearity becomes an even greater challenge because the IIP3 of the final stage must be sufficiently high to accommodate the gain and linearity of the prior stages and avoid impacting the overall linearity. The cascaded linearity of two circuit blocks A and B (ignoring secondary mixing products) can be approximated as

$$\text{IIP3}_{cas}^2 \approx \left[\frac{1}{\text{IIP3}_A^2} + \frac{G_A^2}{\text{IIP3}_B^2} \right]^{-1}, \tag{5}$$

for IIP3_A and IIP3_B corresponding to the IIP3 values of the first- and second-stages, respectively, and G_A denoting the gain of the first-stage [14]. All units are in the linear scale. From this relation it is apparent that the linearity of the second-stage (IIP3_B) needs to be some margin greater than the output-referred IP3 (OIP3 [dBm] = IIP3 + $Gain$) of the first-stage to avoid degrading IIP3_{cas}.

A common figure-of-merit for receiver DR is known as "spurious-free dynamic range" (SFDR), which corresponds to the range of input signal power between the noise floor (F) and the signal level at which the IM3 products exceed the noise floor, and is expressed (in dB) as

$$SFDR = \frac{2(\text{IIP3} - F)}{3} - \text{SNR}_{min}, \tag{6}$$

where SNR_{min} corresponds to the minimum SNR requirements for the system [15].

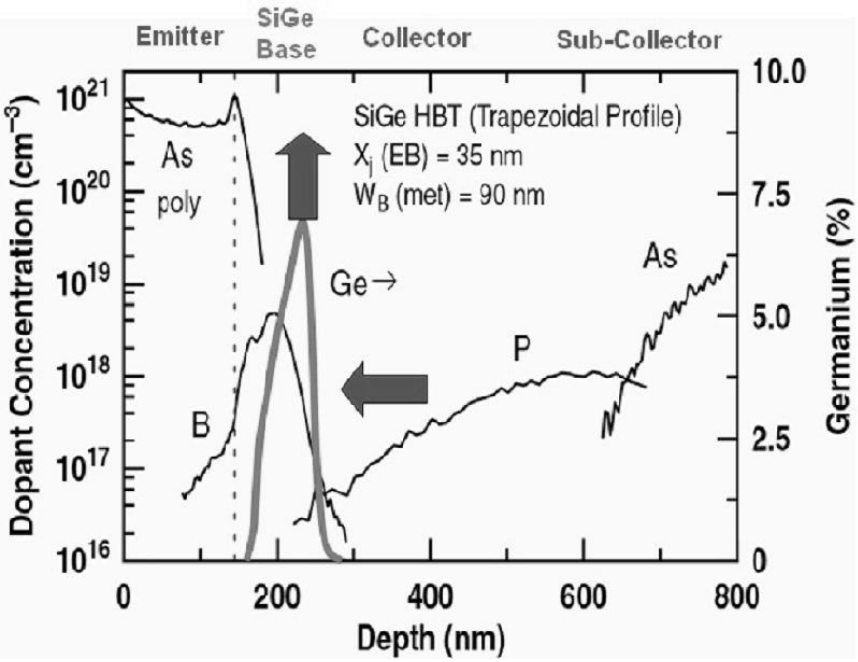

Figure 7: Vertical SIMS profile showing doping concentration and Ge profile within a first generation SiGe HBT [1].

1.2 SiGe HBT BiCMOS Technology

Several generations of SiGe HBT BiCMOS technology exist in commercial production worldwide and are deployed in a wide variety of applications, including cellular handsets, wireless LAN, satellite communications, radar systems, and beyond. The key difference between SiGe HBTs and standard Si BJTs is the inclusion of the compositionally graded SiGe alloy within the boron-doped epitaxial base layer of the NPN transistor. This germanium profile, depicted in the SIMS doping profile of a first-generation SiGe HBT in Figure 7, makes it possible to engineer the energy bandgap in the base region for optimized device performance while maintaining compatibility with standard Si (e.g. CMOS) processes. The Ge layer is typically grown using ultra-high vacuum/chemical vapor deposition (UHV/CVD), allowing for a lower thermal cycle and excellent process control during deposition. This extra process step can be added in modular fashion to standard Si CMOS processes with relatively little impact on CMOS characteristics, fabrication yield, and overall throughput [1].

The vertical self-alignment scheme of the emitter window opening with respect to the extrinsic base region, shown in Figure 8 for a third-generation SiGe HBT, is typically employed in SiGe HBT

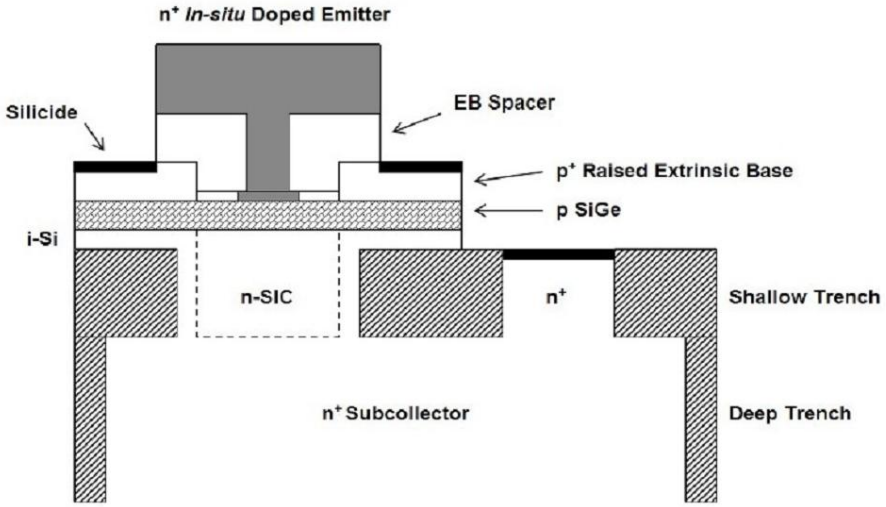

Figure 8: A schematic device cross-section of a third generation BiCMOS SiGe HBT [1].

fabrication because of its several advantages, including reduced parasitics and thin base region. These factors serve to reduce carrier transit time and enable faster device performance. The low thermal budget of UHV/CVD is necessary to maintain a thin base region because of the diffusive nature of boron in silicon. Small amounts of carbon doping may also be included in the active base region to suppress boron out-diffusion and maintain a narrow base profile and enhance device performance [1]. Shallow and deep trench isolation is incorporated in many processes, as shown in Figure 8. Selectively implanted collector (SIC) doping allows devices with different breakdown voltages to be fabricated side by side in a given SiGe HBT technology. In typical processes the NPNs are fabricated in at least two flavors: "high-performance" with high collector doping and low breakdown voltage, and "high-breakdown" with lower collector doping and higher breakdown voltage.

Trans-generational SiGe HBT performance enhancements may be achieved through lateral and vertical scaling and Ge profile optimizations. The SiGe HBT BiCMOS technology generations examined in this thesis are referred to as SiGe 5HP, SiGe 7HP, and SiGe 8HP, and are in commercial production at IBM. Important HBT technology and performance characteristics are summarized in Table 1. At times, these technologies may be referred to by their approximate peak f_T performance: 50 GHz, 120 GHz, and 200 GHz, respectively.

Table 1: Characteristic device parameters for three SiGe BiCMOS technology generations.

SiGe BiCMOS Technology **SiGe HBT Parameters**	IBM 5HP	IBM 7HP	IBM 8HP
Drawn Emitter Width (μm)	0.5	0.2	0.12
peak β	100	200	400
V_A (V)	65	120	> 150
BV_{CEO} (V)	3.3	2.0	1.7
BV_{CBO} (V)	10.5	6.4	5.9
Peak f_T (GHz)	51	120	207
Peak f_{max} (GHz)	69	100	285
min. NF_{min} (dB)	0.8	0.4	< 0.3

Compatibility with state-of-the-art Si CMOS technology is a major feature of the SiGe HBT. In first-generation SiGe 5HP BiCMOS technology, the 100 GHz SiGe HBT paired with 0.35 μm (3.3 V) CMOS. Second-generation SiGe 7HP BiCMOS technology incorporates 0.18 μm (1.8 V) CMOS, while third-generation SiGe 8HP BiCMOS technology includes 0.12 μm (1.2 V) CMOS.

1.3 Device Physics of SiGe HBTs

The SiGe HBT technology utilizes bandgap engineering of the SiGe base in order to increase the performance of the bipolar transistor terms of higher speed, higher current gain, higher linearity, and lower noise. A well-engineered Ge profile can effectively decouple key device parameters that otherwise lead to critical performance trade-offs in standard Si BJT devices.

From a physical perspective, the crystalline lattice constants differ between Si and Ge, and as a result, a SiGe alloy naturally has a slightly larger lattice constant than does Si. This lattice mismatch results in compressive straining on the SiGe layer grown pseudomorphically on Si. Therefore, for a given Ge concentration, the SiGe film must be thinner than a certain critical value to retain thermodynamic stability and avoid relaxation defects. The compressive strain in the SiGe film also results in carrier mobility enhancement and aids in transport properties of the device.

Because the energy bandgap of Ge (0.66 eV at 300K) is considerably smaller than that of Si (1.12 eV at 300K), the bandgap in a SiGe alloy is effectively tunable by the Ge concentration (reduced by approximately 7.5 meV per 1% Ge), insofar as thermodynamic stability allows [1]. The energy band diagram for a standard Si BJT and a comparable SiGe HBT, biased in forward active mode, is shown in Figure 9. The effect of the graded Ge profile in the base region is apparent

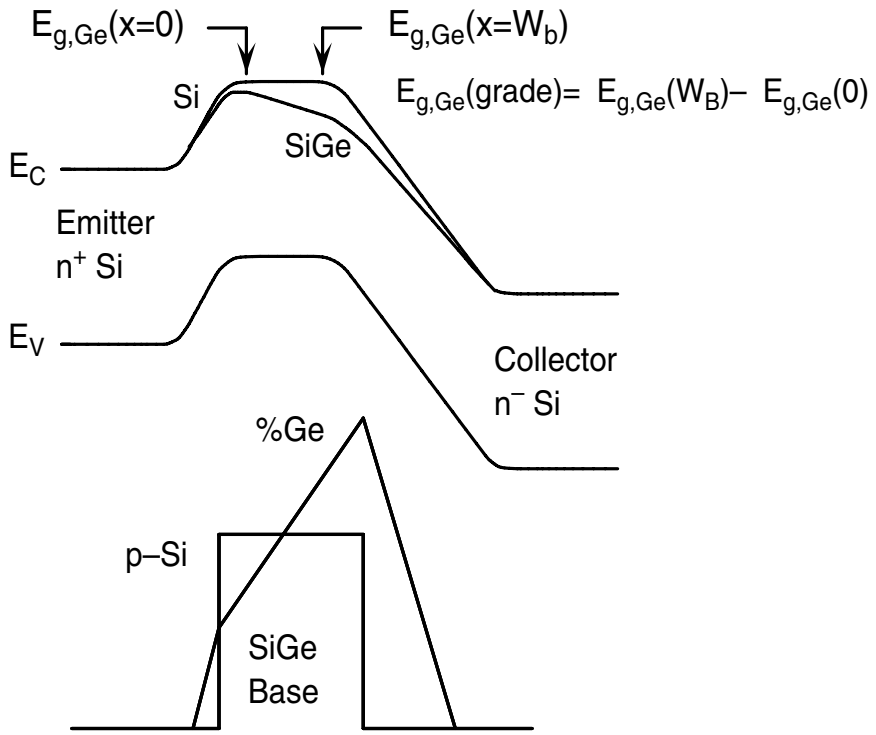

Figure 9: Energy band diagram for a graded base SiGe HBT and a Si BJT [1].

in the offset between the respective conduction bands. As a result, the potential barrier for minority carrier injection into the base region is reduced for a given V_{BE}, resulting in increased collector current density (J_C) and thus increased gain for the SiGe device. This result can be physically expressed using the generalized Moll-Ross relation for collector current density [16],

$$J_C = \frac{q(e^{qV_{BE}/kT-1})}{\int_0^{W_b} \frac{p_b(x)dx}{D_{nb}(x)n_{ib}^2(x)}}. \tag{7}$$

Solving the integral in the denominator requires an equation that relates the Ge-induced offset of the bandgap to the intrinsic carrier concentration as a function of position, which can be written as

$$n_{ib}^2 = \gamma n_{io}^2 e^{\Delta E_{gb}^{app}/kT} e^{[\Delta E_{g,Ge}(grade)]x/(W_b kT)} e^{\Delta E_{g,Ge}(0)/kT}, \tag{8}$$

where $\Delta E_{gb}^{app}/kT$ is the apparent bandgap narrowing resulting from heavy doping in the base. The low-doping intrinsic carrier density for Si is $n_{io}^2 = N_C N_V e^{-E_{go}/kT}$, and $\gamma = (N_C N_V)_{SiGe}/(N_C N_V)_{Si}$ represents the effective density-of-states ratio (< 1) between SiGe and Si [17]. Combining Equations 7 and 8, and assuming a linearly graded Ge profile ($\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0)$)

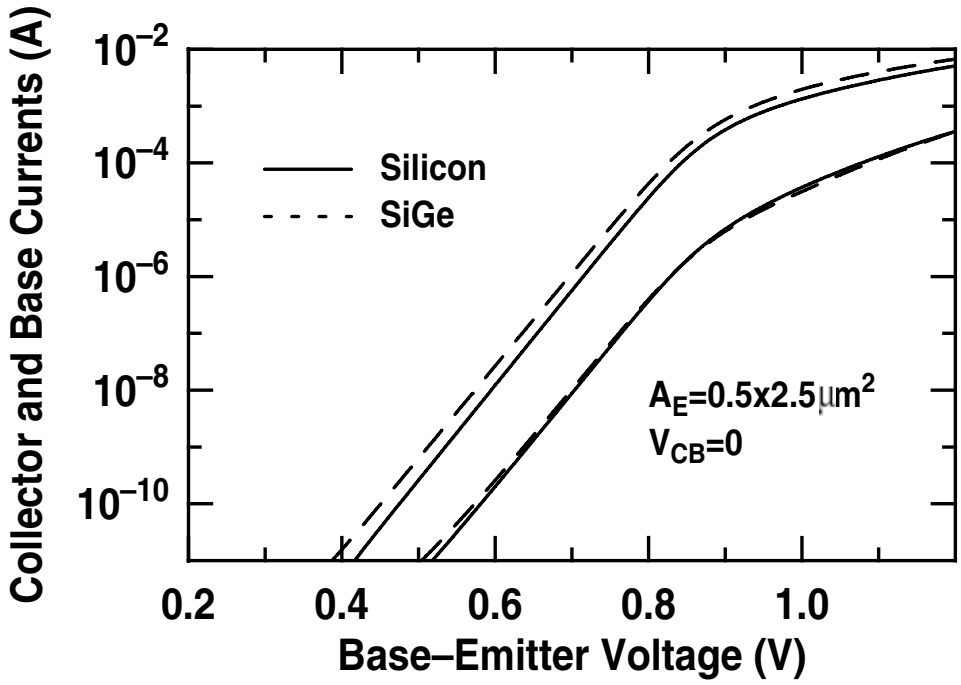

Figure 10: Representative Gummel plot for a SiGe HBT as compared to a Si BJT [1].

yields an overall expression for collector current density (J_C) in a SiGe HBT [18],[19]:

$$J_{C,SiGe} = \frac{qD_{nb}}{N_{ab}^{-}W_b}\left(e^{qV_{BE}/kT}-1\right)n_{io}^2 e^{\Delta E_{gb}^{app}/kT}\left\{\frac{\widetilde{\gamma}\widetilde{\eta}e^{\Delta E_{g,Ge}(0)/kT}\Delta E_{g,Ge}(grade)/kT}{1-e^{-\Delta E_{g,Ge}(grade)/kT}}\right\} \qquad (9)$$

where the symbol "$\sim$" denotes a position-averaged quantity, N_{ab}^{-} is the ionized doping level in the base, and $\tilde{\eta} = \left(\widetilde{D_{nb}}\right)_{SiGe}/(D_{nb})_{Si}$ is the minority electron diffusivity ratio (> 1) between SiGe and Si. The influence of the Ge-induced energy band offset on collector current density is contained entirely in the bracketed term in Equation 9 and thus can be described as the SiGe current gain enhancement factor:

$$\frac{\beta_{SiGe}}{\beta_{Si}} \cong \frac{J_{C,SiGe}}{J_{C,Si}} = \frac{\widetilde{\gamma}\widetilde{\eta}\Delta E_{g,Ge}(grade)/kTe^{\Delta E_{g,Ge}(0)/kT}}{1-e^{-\Delta E_{g,Ge}(grade)/kT}}. \qquad (10)$$

This relation demonstrates that Ge-induced energy band offset at the EB junction ($\Delta E_{g,Ge}(0)$) exerts an exponential influence on the gain increase of the device. This enhancement is depicted in Figure 10, which compares the Gummel characteristics for a typical SiGe HBT and a similarly constructed Si BJT. The SiGe HBT clearly exhibits higher collector current with approximately the same base current as the Si BJT and hence increased current gain.

In the case of "strong Ge grading" ($\Delta E_{g,Ge}(grade) >> kT$), characteristic of a triangular Ge profile, the exponential term on the denominator becomes very small and Equation 10 approximately reduces to $(\widetilde{\gamma}\widetilde{\eta}\Delta E_{g,Ge}(grade)/kT)e^{\Delta E_{g,Ge}(0)/kT}$. In the case of "weak Ge grading" ($\Delta E_{g,Ge}(grade)$ $<< kT$), as in a box Ge profile, the SiGe current gain enhancement factor is shown to be approximately $\widetilde{\gamma}\widetilde{\eta}e^{\Delta E_{g,Ge}(0)/kT}$.

In addition to current gain (β), the output conductance ($\partial I_C/\partial V_{CE}$ at fixed V_{BE}) of a transistor is a key consideration in analog design. This factor is equivalently described using the output resistance r_o, with output conductance equal to $1/r_o$, and an ideal transistor possesses infinite output resistance. However, real transistors possess finite values of r_o, caused in large part in bipolar devices by what is referred to as the "Early Effect." This effect occurs as V_{CB} increases, which causes backside depletion on the neutral base. The effective width of the active base region is therefore reduced, which increases the minority carrier (electron) concentration gradient across the base and increases the collector current. This behavior is commonly characterized using an experimental parameter known as the Early Voltage (V_A):

$$V_A = J_C(0)\left\{\left.\frac{\partial J_C}{\partial V_{CB}}\right|_{V_{BE}}\right\}^{-1} - V_{BE} \approx \left\{\left.\frac{\partial J_C}{\partial W_b}\right|_{V_{BE}}\frac{\partial W_b}{\partial V_{CB}}\right\}^{-1}. \tag{11}$$

Therefore, the V_A enhancement ratio between a comparable SiGe HBT and Si BJT can be written as

$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} = e^{\Delta E_{g,Ge}(grade)/kT}\left[\frac{1-e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right], \tag{12}$$

which shows the exponential influence of the Ge-induced bandgap grading on the Early voltage [1]. Thus, the Ge profile in a SiGe HBT provides separate "levers" for optimizing β and V_A ($\Delta E_{g,Ge}(0)$ and $\Delta E_{g,Ge}(grade)$, respectively). In standard Si BJTs, enhancement of one of these two factors fundamentally requires degradation of the other, since they both are related to the base doping. But with the effective decoupling of β and V_A from base doping using a well-constructed Ge profile, this trade-off is sidestepped and the overall $\beta \cdot V_A$ product of a SiGe HBT is substantially higher than that of an otherwise similar Si BJT [1].

SiGe HBTs also show substantial improvement in *ac* performance over conventional Si BJTs, allowing SiGe HBTs to achieve frequency response suitable for many high-frequency RF and millimeter wave applications. The base transit time (τ_b) constitutes a significant portion of the total

transport delay time for carriers in bipolar devices and thus can be a limiting factor in overall *ac* performance. A graded Ge profile induces a drift field in the neutral base that accelerates minority carriers and reduces τ_b. This enhancement to can be expressed as [1]

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\widetilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[1 - e^{-\Delta E_{g,Ge}(grade)/kT} \right] \right\}. \tag{13}$$

Additionally, since the emitter charge storage delay time (τ_e) is proportional to $1/\beta$, the Ge enhancement to this factor can be written from Equation 10 as

$$\frac{\tau_{e,SiGe}}{\tau_{e,Si}} \simeq \frac{J_{C,Si}}{J_{C,SiGe}} = \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\widetilde{\gamma}\widetilde{\eta} \frac{\Delta E_{g,Ge}(grade)}{kT} e^{\Delta E_{g,Ge}(0)/kT}}. \tag{14}$$

A standard figure-of-merit for dynamic transistor performance is the unity-gain cutoff frequency (f_T). For low-injection, this parameter can be expressed as

$$f_T = \frac{1}{2\pi} \left[\frac{1}{g_m}(C_{eb} + C_{cb}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{cb} \right]^{-1}, \tag{15}$$

so reducing τ_b and τ_e will result in higher f_T. Likewise, the unity power-gain frequency (or, maximum oscillation frequency, f_{max}) will also improve since it is related to f_T by

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb} r_b}}. \tag{16}$$

Therefore, the Ge grading in the base region of the SiGe HBT significantly improves both f_T and f_{max}, and thus overall *ac* performance.

1.4 Objective and Contributions of This Work

This work investigates the fundamental device limits related to operational voltage constraints and linearity in state-of-the-art silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) in order to support the design of robust next-generation high-frequency transceivers. This objective requires a broad understanding of how much "usable" voltage exists compared to conventionally defined breakdown voltage specifications, so the role of avalanche-induced current-crowding (or "pinch-in") effects on transistor performance and reliability are carefully studied. Also, the effects of intermodulation distortion are examined at the transistor-level for new and better understanding of the limits and trade-offs associated with achieving enhanced dynamic range and linearity performance on existing and future SiGe HBT technology platforms. Based on these investigations, circuits designed for superior dynamic range performance are presented.

New contributions to the field made by this work may be summarized by the following items.

1. The first-ever comprehensive analysis of the effects of scaling and bias on operating voltage constraints in advanced SiGe HBTs (Chapter 3, also published in [20]).

2. Novel analysis of factors contributing to common-base (CB) avalanche instabilities in SiGe HBTs (Chapter 3, also published in [21]).

3. An investigation of operating voltage constraints for SiGe HBTs operating in extreme environments for space-borne electronics applications (Chapter 3, also published in [22], [23]).

4. Experimental analysis of large-signal RF performance, linearity, and reliability of cascode SiGe HBTs under aggressive collector voltage bias conditions for power amplifier (PA) applications (Chapter 4, also published in [24]).

5. Novel investigation of high-power RF operating limits for cascode SiGe HBTs, with new expressions for large-signal safe-operating area supported by experimental data (Chapter 4, also published in [25]).

6. Investigation of common-base intermodulation distortion with new expressions for linearity performance derived from Volterra series analysis (Chapter 5, also published in [26]).

7. Design and analysis of a high gain, high-linearity X-band two-stage low-noise amplifier with sub-2 dB noise figure for enhanced dynamic range performance (Chapter 6, also published in [27]).

8. Design and analysis of a 0.25-Watt X-band cascode power amplifier that achieves improved power density using aggressive collector voltage bias (Chapter 6).

CHAPTER II

PHYSICS OF BIPOLAR BREAKDOWN

2.1 Introduction

Avalanche multiplication and breakdown effects represent a critical component in the study of operating voltage limits and dynamic range of SiGe HBTs, particularly as these transistors are scaled to operate at higher frequencies. This chapter will review the fundamental physics of bipolar breakdown, and highlight important definitions and relations that serve as the basis for the experimental study of operating limits and large-signal dynamic range presented in this thesis.

2.2 Avalanche Multiplication

Typically the SiGe HBT is operated in the forward-active mode, in which case its collector-base junction is under reverse voltage bias. As with any reverse biased p-n junction, this reverse voltage will increase the electric field in the collector-base depletion region, sweeping free electrons toward the collector-side and free holes toward the base-side of the junction. During this process, a carrier in the depletion region may undergo a collision event with the semiconductor lattice. For low reverse voltage bias the electric field in the depletion region is weak. In this case carriers in the depletion region obtain only relatively low kinetic energy that is absorbed by the lattice as a phonon upon collision. However, increasing the magnitude of the reverse bias will increase the electric field, causing carriers in the depletion region to obtain substantially higher energy. In the event that an electron of sufficient velocity collides with the lattice, excess energy may be transferred to an electron in the valence band, promoting this carrier to the conduction band and creating an electron-hole pair (EHP). This generation process is the inverse of the Auger effect, and is known as impact ionization [28]. An electron generated during an impact ionization event itself may undergo a lattice collision and generate an additional EHP, and so on, as illustrated in Figure 11. This "snowballing" phenomenon of impact-ionized carriers is referred to as avalanche multiplication.

As the reverse bias potential across the junction (V_{CB} in a bipolar transistor) increases, the probability that each carrier in the depletion region will undergo an impact ionization event increases,

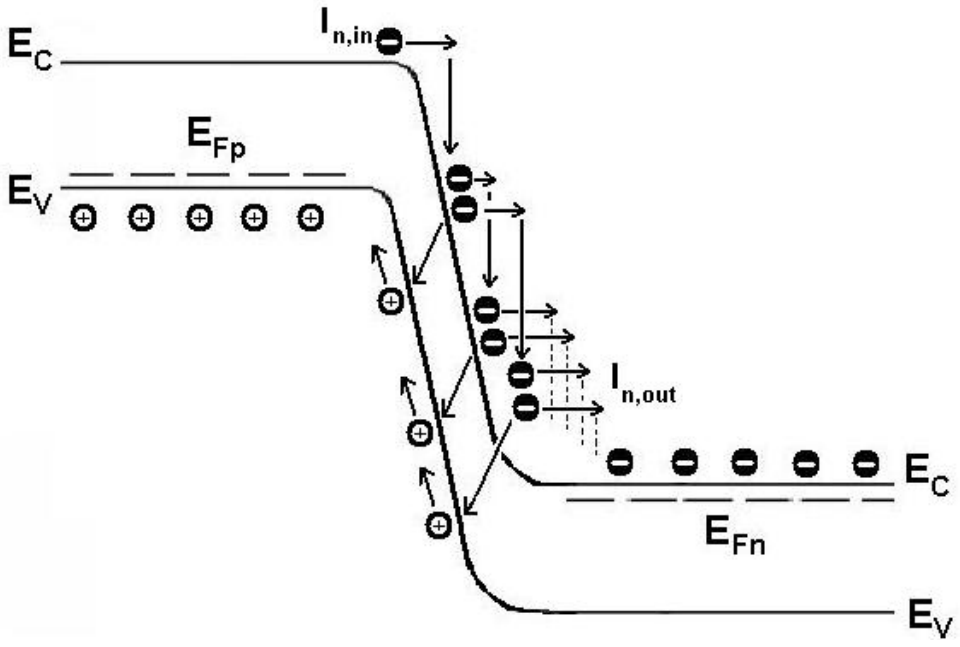

Figure 11: Schematic illustration of the avalanche multiplication process in a reversed bias p-n junction.

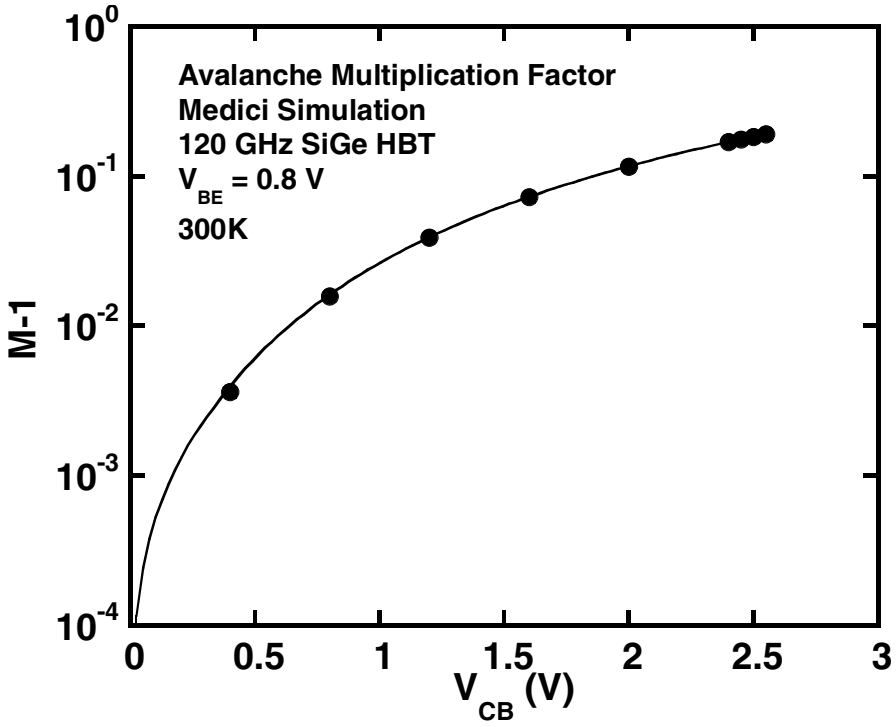

Figure 12: MEDICI device simulation of a 120 GHz SiGe HBT showing the avalanche multiplication factor ($M - 1$) as a function of collector voltage.

eventually leading to junction breakdown. This probability is typically represented as the avalanche multiplication factor (M), which is the ratio of reverse-biased junction current excluding impact ionization to the junction current including impact ionization, or

$$M = I_{n,out}/I_{n,in} \tag{17}$$

for $I_{n,in}$ being the electron current entering the collector-base depletion region and $I_{n,out}$ being the electron current exiting this depletion region (equal to the current at the collector terminal for the bipolar device). A physical model for avalanche multiplication can be expressed in terms of the position-dependent electric field ($E(x)$) in the depletion region as

$$M = 1 + \int_0^W \alpha_n e^{-E_{crit}/E(x)} dx \tag{18}$$

where W is the depletion region width, α_n is the election ionization coefficient, and E_{crit} is the critical electric field [29]. Avalanche breakdown of the junction is defined as the condition where M approaches infinity. When this occurs, the collector current (I_C) will approach infinity unless externally limited. For bipolar devices, the voltage at which the collector-base junction undergoes reverse breakdown is designated as BV_{CBO} (open-emitter breakdown voltage), and represents the absolute maximum collector voltage of a transistor. This important figure-of-merit is given in Table 1 for the 50, 120, and 200 GHz SiGe HBT technologies.

Given BV_{CBO}, an empirical relation known as the Miller Approximation expresses the voltage (V_{CB}) dependence of the avalanche multiplication factor as

$$M = \frac{1}{1 - (V_{CB}/BV_{CBO})^m} \tag{19}$$

where m is a fitting parameter [30]. The avalanche multiplication factor for a SiGe HBT can be extracted from standard *dc* measurements [31]. This parameter is commonly plotted as (log) $M - 1$ verses (linear) collector-base voltage (V_{CB}), as shown in Figure 12 for a MEDICI simulation of a 120 GHz SiGe device.

For simplicity, in many cases $M - 1$ for a given V_{CB} is treated as a constant with respect to collector current density (J_C), and for low injection this approximation is usually acceptable. However, it is well known that at high injection, $M - 1$ shows a stronger dependence on J_C because of high carrier charge concentration reducing the effective doping (and thus the effective electric field)

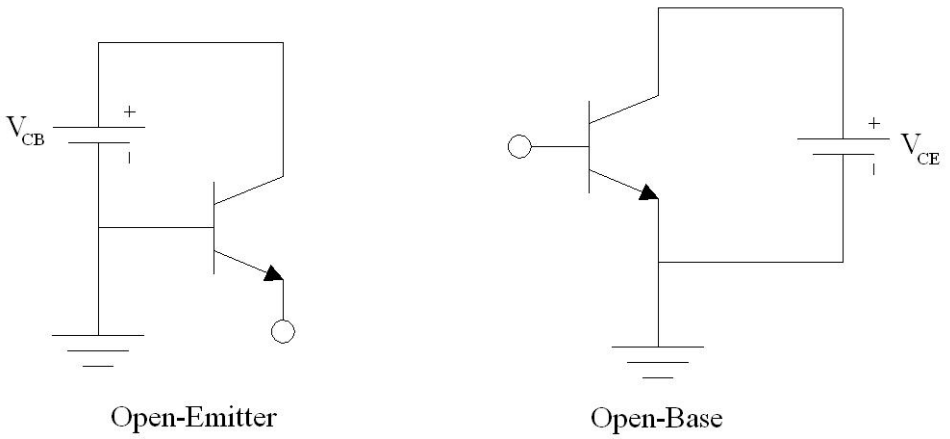

Figure 13: Open-emitter (CBO) and open-base (CEO) *dc* bias configurations.

within the collector-base depletion region [1]. Also, $M - 1$ has a negative temperature coefficient because of phonon scattering, which absorbs energy during carrier-lattice collisions and reduces the probability of EHP creation, and changes in carrier mean free path [29]. Therefore, self-heating effects that occur at high-current densities will serve to reduce avalanche multiplication. Conversely, breakdown effects can be expected to worsen for low-temperature (cryogenic) operating conditions because of increased $M - 1$.

2.3 Open-Base Breakdown

In addition to the open-emitter breakdown voltage (BV_{CBO}), the open-base breakdown voltage (BV_{CEO}) serves as another important bipolar figure-of-merit. The open-emitter and open-base configurations are shown in Figure 13. In contrast to the open-emitter configuration, the very high external impedance at the base terminal for the open-base configuration prevents holes generated by avalanche multiplication from exiting the base terminal, causing these carriers to be injected into the emitter. For a current gain of β, this results in an emitter current

$$I_E = (\beta + 1)(M - 1)I_{n,in}. \tag{20}$$

However, $I_{n,in}$ will increase as I_E increases, since

$$I_{n,in} = I_E \left(1 - \frac{1}{\beta + 1}\right), \tag{21}$$

resulting in a positive feedback loop that will cause premature breakdown for the open-base configuration.

The role of this positive feedback on open-base breakdown is demonstrated when the collector and base currents are expressed including avalanche effects:

$$I_C = M \cdot \beta I_{Bsat}(e^{V_{BE}/V_T} - 1) + M \cdot I_{CBO} \tag{22}$$

and

$$I_B = I_{Bsat}(e^{V_{BE}/V_T} - 1) - \beta(M-1) \cdot I_{Bsat}(e^{V_{BE}/V_T} - 1) - M \cdot I_{CBO} + I_{SE}(e^{V_{BE}/n_E V_T} - 1) \tag{23}$$

where βI_{Bsat} is the transistor saturation current, I_{CBO} is the collector-base leakage current, I_{SE} is the reverse emitter-base junction saturation current, and n_E is the emitter-base junction ideality factor [32].

Solving Equation 23 for I_{Bsat} with $I_B = 0$ and substituting this result into Equation 22 shows that the collector current under open-base conditions is

$$I_C = \frac{M((\beta+1)I_{CB0} - \beta \cdot I_{SE}(e^{V_{BE}/n_E V_T} - 1))}{(1 - \beta(M-1))}. \tag{24}$$

This expression shows that the collector current with approach infinity as the denominator approaches zero. Thus, the condition for open base breakdown (BV_{CEO}) is

$$\beta(M-1) = 1 \tag{25}$$

and will occur at considerably lower V_{CE} than BV_{CBO}, as reflected in Table 1. In many SiGe technologies, the ratio between the two breakdown voltages has been observed to be approximately one-third [13].

2.4 Base Current Reversal and Pinch-In Effects

When the base terminal of the bipolar transistor is connected to ground (common-base configuration) or driven by a low-impedance (e.g. *voltage*) source, holes generated by avalanche multiplication are free to exit the base, which results in a reduction in the base current as Equation 23 indicates. As $(M-1)$ increases, this will cause I_B to be reduced until it reaches zero and reverses sign. This phenomena is referred to as *base current reversal* (BCR). Equation 23 shows that I_B will equal zero

when $\beta(M-1))=1$, identical to the condition for open-base breakdown [32] [33]. In this case the I_{CBO} and I_{SE} terms are much smaller than the I_{Bsat} terms and can be neglected. Therefore, BCR will occur when the product of the avalanche multiplication factor and the *dc* current gain exceeds unity, or

$$\beta(M-1)>1. \tag{26}$$

High levels of reverse base current may cause constriction of current flow within the transistor, which results in unstable device behavior. These current flow non-uniformities are referred to as "pinch-in" effects. Starting with a few basic assumptions, this section provides a simplified and qualitative examination of pinch-in-related phenomena.

To illustrate the origin of the pinch-in effect, consider a simplified one-dimensional horizontal cross section through the neutral base of a transistor with two extrinsic base contacts on either side of the emitter window (as shown in Figure 8). The active device is assumed to be horizontally symmetrical about the center of the neutral base region, denoted as position $x=0$. Therefore, for drawn emitter width W_E, the boundaries of the active base occur at $x=+W_E/2$ and $x=-W_E/2$. Initially it is assumed that current distribution I_E is uniform within the device. Therefore, the current passing within the small segment between x and $x+\delta x$ is simply a constant with respect to position, or

$$\delta I_E(x)=\delta I_E=\frac{I_E}{W_E}. \tag{27}$$

This scenario is depicted in Figure 14. The excess current generated by impact ionization in the collector-base depletion region can be written as

$$I_{AVC}=\frac{I_E}{(\beta+1)}[(M-1)\beta-1]\approx(M-1)I_E \tag{28}$$

for current gain $\beta>>1$. Likewise, assuming for strong BCR that the product $(M-1)\beta>>1$, the forward injected hole current at the base is very small compared to I_{AVC} and can be neglected. The avalanche current consists of both an electron current component, which is swept into the collector, and a hole current component, which is swept into the base. Therefore, the avalanche hole current generated within the small segment between x and $x+\delta x$ within the base region is

$$\delta I_{AVC}(x)\approx\frac{(M-1)I_E}{W_E}. \tag{29}$$

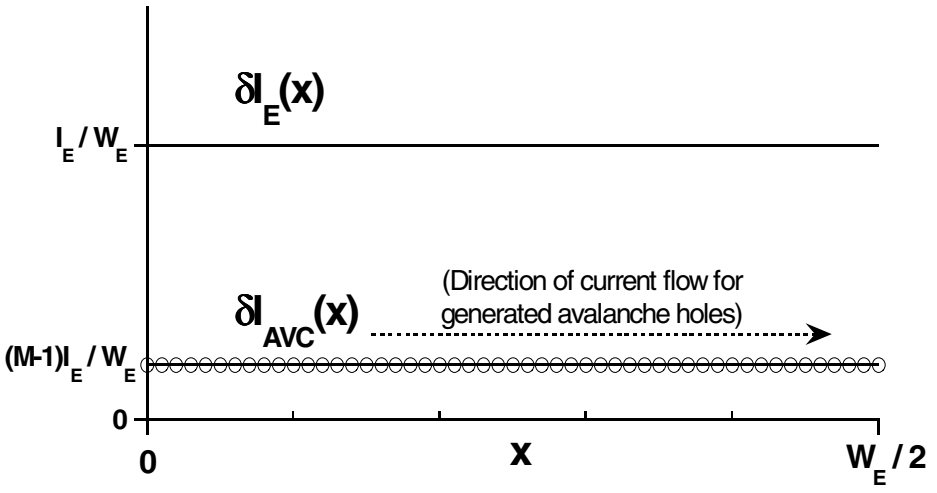

Figure 14: Simplified depiction of injected current (units: A/μm) and avalanche generation as a function of position within the device.

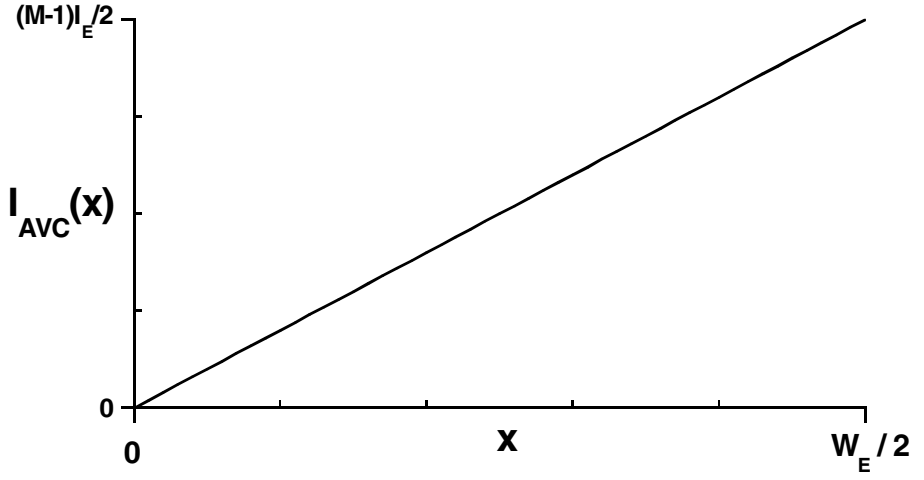

Figure 15: Simplified depiction of avalanche current (units: A) as a function of position within the active device.

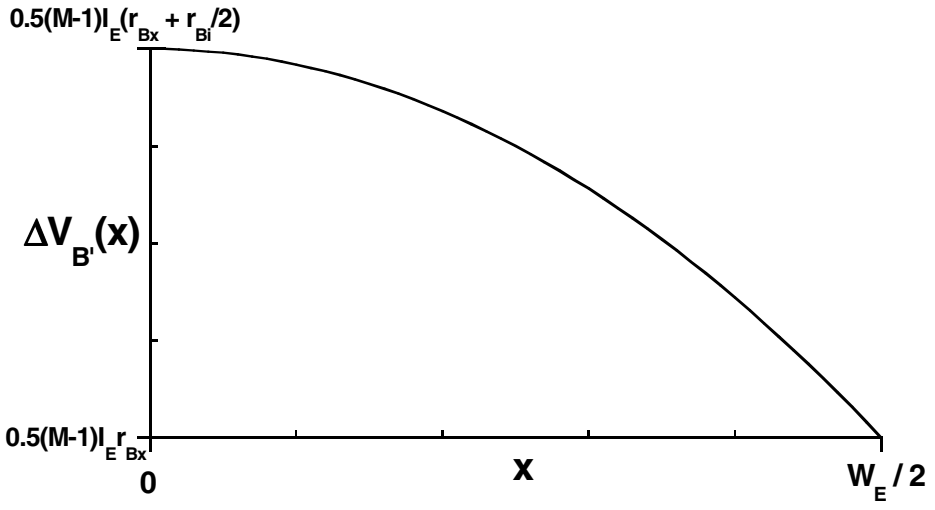

Figure 16: Simplified depiction of intrinsic base potential (units: V) as a function of position within the active device.

Assuming the base current (I_B) is not fixed externally, the excess holes generated by avalanche multiplication will flow from their point of origin ($0 < x < W_E/2$) to the extrinsic base boundary ($x = W_E/2$) and exit through the base terminal. The total avalanche current at a particular point x within the base is the summation of the generated avalanche current for each small segment δx between the center of the device ($x = 0$) and the position x and therefore can be represented as

$$I_{AVC}(x) = \int_0^x \delta I_{AVC}(y)dy \approx \frac{(M-1)I_E}{W_E}x, \tag{30}$$

which is plotted in Figure 15. Clearly, the hole current is vanishingly small at the center of the symmetric device, and equals half of the total avalanche current at $x = +W_E/2$. The remaining half of the avalanche current exits through the other extrinsic base contact at $x = -W_E/2$. For the voltage at the base terminal V_B, the intrinsic base potential is defined with respect to a position-dependent offset voltage as $V_{B'} = V_B + \Delta V_{B'}$. Treating the intrinsic base resistance (r_{Bi}) as a uniformly distributed factor yields $\delta r_{Bi}(x) = \delta r_{Bi} = \frac{r_{Bi}}{W_E/2}$. Therefore, the position-dependent intrinsic offset voltage can be written as

$$\Delta V_{B'}(x) = \int_x^{W_E/2} \delta r_{Bi} I_{AVC}(y)dy. \tag{31}$$

Substituting the result from Equation 30 into Equation 31, and assuming a potential drop across

the extrinsic base resistance is equal to $r_{Bx}I_{AVC}(0)$, results in the expression

$$\Delta V_{B'}(x) = \frac{r_{Bi}(M-1)I_E}{4} - r_{Bi}(M-1)I_E(x/W_E)^2 + r_{Bx}(M-1)I_E/2, \tag{32}$$

as plotted in Figure 16. At this point the initial assumption of uniform current distribution must be reconsidered, given that the injected electron current (I_{C0} is a function of intrinsic base potential $V_{B'E'}(x)$, according to

$$I_{C0} = I_S e^{V_{B'E'}/(kT/q)} \tag{33}$$

Therefore, for saturation current I_S and $I_E = \frac{\beta}{\beta+1} I_{C0} \approx I_{C0}$, the position-dependent emitter current can be written as

$$\delta I_E(x) = I_E(x)/W_E \approx \frac{I_S}{W_E} e^{V_{B'E'}(x)/(kT/q)}. \tag{34}$$

Ignoring the potential drop across the parasitic emitter resistance (r_E), $V_{B'E'}(x)$ can be replaced with $V_{BE} + \Delta V_{B'}(x)$. The thermal voltage is defined as $V_T = kT/q$. Thus, for nonuniform I_E distribution, Equation 31 becomes

$$\Delta V_{B'}(x) = \int_x^{W_E/2} \left[\frac{2r_{Bi}}{W_E^2}(M-1)I_S e^{V_{BE}/V_T} \right] e^{\Delta V_{B'}(y)/V_T} y dy. \tag{35}$$

The terms enclosed within the brackets may be treated as a constant factor. It is clear, however, that the change in intrinsic base potential ($\Delta V_{B'}(x)$) is an exponential function of itself and that this integral must be solved iteratively. Forgoing that, this expression demonstrates the positive-feedback mechanism associated with pinch-in, indicating that the intrinsic base potential distribution is stable for $\Delta V_{B'} << V_T$ and unstable as $\Delta V_{B'}$ becomes substantial compared V_T, at which point pinch-in occurs. Considering the voltage drop across the emitter resistance (r_E), then $V_{B'E'}(x) = V_{BE} + \Delta V_{B'}(x) - \Delta V_{E'}(x)$. Clearly, this additional term produces a stabilizing effect (negative feedback), particularly as the emitter current increases, and will be addressed from an experimental side in the sections to follow.

Two-dimensional device simulations were performed using MEDICI, including hydrodynamic energy balance and impact ionization models, for various values of V_{CB}. Figure 17, taken from these simulations, shows the onset of distributed current and voltage non-uniformities within a cross section of the active base region. The relevant device profile is aligned with the spatial dimensions of

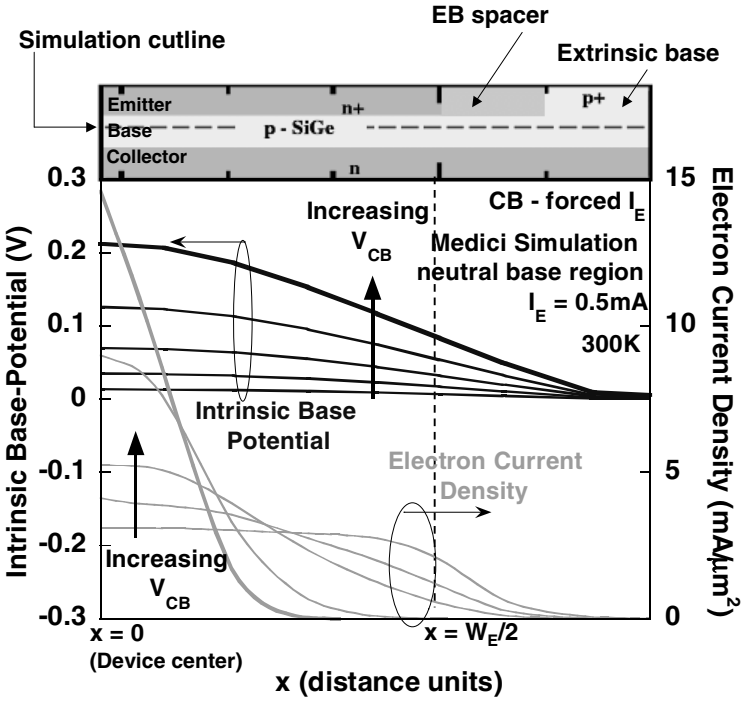

Figure 17: MEDICI simulation of a 120 GHz SiGe HBT showing the intrinsic potential distribution and onset of current constriction within the neutral base.

the plot in the inset above Figure 17, and the examined cross section is highlighted. These simulated results are very similar to the intrinsic base voltage characteristics predicted by Equation 32.

Overall, the severe current localization associated with pinch-in produces unstable behavior related to self-heating and electric field collapse [34]. These instabilities present undesirable conditions for device biasing and operation. Moreover, this behavior is not captured by standard device models (such as VBIC or HICUM) used for circuit simulations. Therefore, understanding the role of pinch-in effects in SiGe HBTs is extremely important for ensuring reliable device and circuit operation.

2.5 Role of Collector Design

The collector design of the SiGe HBT plays an important role in both the speed and the breakdown performance of the transistor. As demonstrated in Equation 15, as τ_b and τ_e are reduced, the time delays attributed to the parasitic capacitances within the device become more significant. An increase in collector current density (J_C) is required to decrease the charging times of the parasitic capacitances (C_{eb} and C_{cb}). Therefore, increased J_C is a common characteristic associated with

technology scaling and f_T optimization in SiGe HBTs, as shown in Figure 1.

At high J_C, carriers in the collector-base space charge region (CB-SCR) will compensate the local ionized charge, leading to a collapse of the electric field in this region. As a result, the base region will "push-out" into the CB-SCR (the Kirk effect), decreasing the current gain and degrading the performance of the transistor. Therefore, in order to operate at high J_C, higher collector doping is required to suppress the Kirk effect. Increasing the collector doping will increase the magnitude of the drift field within the depletion region, thereby increasing avalanche multiplication and reducing the breakdown voltage.

Thus, SiGe HBTs encounter an inherent trade-off between peak f_T and breakdown voltage. This trade-off is reflected in Table 1, which shows that BV_{CBO} decreases from 10.5 V to 5.5 V over the three technology generations as peak f_T increases from 50 GHz to 200 GHz. The product of the breakdown voltage and the peak f_T is a figure-of-merit commonly used to gauge the overall transistor performance. This fundamental limit is more accurately described by the (larger) $BV_{CES} \cdot f_T$ product ($BV_{CES} \approx BV_{CBO}$) than the traditional $BV_{CEO} \cdot f_T$ product [4]. Also, the open-base and pinch-in ($V_{CB-crit}$) voltage limits for SiGe HBTs are likewise decreasing with f_T, as illustrated in Figure 2. Overall, the ever-decreasing operating voltage limits of scaled SiGe HBTs expose new challenges and reveal the growing importance of breakdown-related issues, particularly in the realm of mixed-signal circuit design.

CHAPTER III

DC OPERATING LIMITS IN SIGE HBTS

3.1 Introduction

As discussed already, the breakdown voltages (BV_{CEO}, BV_{CBO}) of SiGe HBTs can be expected to become lower as their high-frequency performance improves. As a result, circuit designers are faced with increasingly stringent device operating restrictions as maximum limits of usable collector voltage are compressed. However, BV_{CEO} and BV_{CBO} do not tell the full story of breakdown voltage constraints, and achieving optimal performance may require the device to operate in the region between these two breakdown voltages. Moreover, the operating limits related to breakdown voltage can vary considerably depending on the bias configuration and the *dc* current drive. Therefore, comprehensive understanding of these limits is crucial to ensure stable and reliable device operation.

A variety of aspects related to the voltage operating limits of state-of-the-art SiGe HBTs are examined in this chapter. Section 3.2 presents experimental results for breakdown voltage limits characterized for different bias configurations and across several technology generations. The role of pinch-in effects, particularly in the common-base (CB) configuration, are examined in Section 3.3. A new analysis approach is introduced to provides a straightforward physical description of pinch-in and identify the key parameters that influence its bias dependence. Section 3.4 addresses the role that extreme environments, such as cryogenic operation and radiation effects, on operating voltage limits.

3.2 Breakdown Characteristics with Technology Scaling

3.2.1 Experimental Overview

In this study, samples from three generations of commercially-available SiGe HBT technology were measured for various *dc* bias conditions to examine the role of technology scaling on breakdown effects and operating voltage limits. These measurements were performed on-wafer using an Agilent 4155C Semiconductor Parameter Analyzer. For each technology node, the standard-performance

Table 2: Relevant breakdown parameters for the HS devices for three SiGe BiCMOS technology generations.

SiGe BiCMOS Technology **SiGe HBT BV Parameters**	1st generation (IBM 5HP)	2nd generation (IBM 7HP)	3rd generation (IBM 8HP)
BV_{CEO} (V)	3.3	2.0	1.7
BV_{CBO} (V)	10.5	6.4	5.9
peak f_T (GHz)	51	120	207
J_C at peak f_T (mA/μm^2)	1.3	5.0	12

Table 3: Relevant breakdown parameters for the HB devices for three SiGe BiCMOS technology generations.

SiGe BiCMOS Technology **SiGe HBT BV Parameters**	1st generation (IBM 5HP)	2nd generation (IBM 7HP)	3rd generation (IBM 8HP)
BV_{CEO} (V)	5.5	4.7	3.5
BV_{CBO} (V)	14	13	12
peak f_T (GHz)	27	27	57
J_C at peak f_T (mA/μm^2)	0.34	0.30	1.4

(HS) devices and the high-breakdown (HB) devices were both characterized in order to study the role of collector design on breakdown performance. The standard-performance HBTs are exposed to additional collector implant (the *selectively implanted collector*, or SIC) resulting in a higher level of n-type doping in the collector region compared to the high-breakdown HBTs. As a result, the HS devices have higher peak f_T and the onset of the Kirk effect occurs at higher collector current density (J_C). Also the breakdown voltage is considerably lower than the HB devices. A snapshot of the relevant breakdown voltage parameters for the standard- and high-breakdown devices is provided in Tables 2 and 3, respectively.

Figures 18 and 19 show the avalanche multiplication factor ($M-1$) measured for the HS and HB devices across the three SiGe HBT technologies generations studied. These results show a strong increase in $M-1$ as the technology is scaled from the first- to the third-generation, which leads to the lower breakdown voltages. In addition, for a given collector voltage (V_{CB}), $M-1$ tends to be at least an order of magnitude higher in the HS devices compared to the respective HB devices. The operating voltage limits across different bias configurations are strongly affected by these differences in the avalanche multiplication rate.

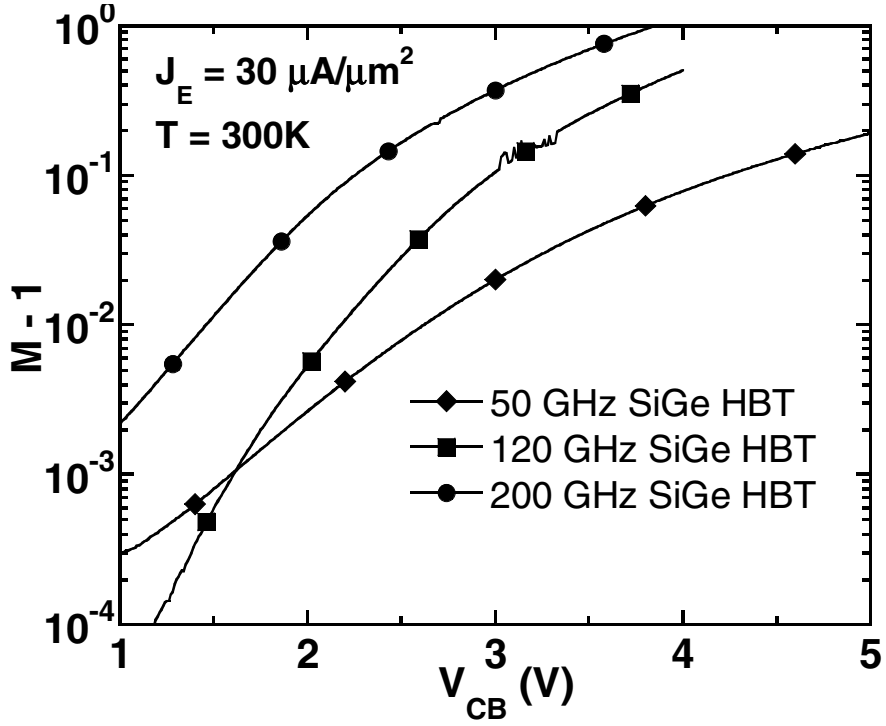

Figure 18: $M - 1$ characteristics for HS devices from three generations of SiGe HBT technology.

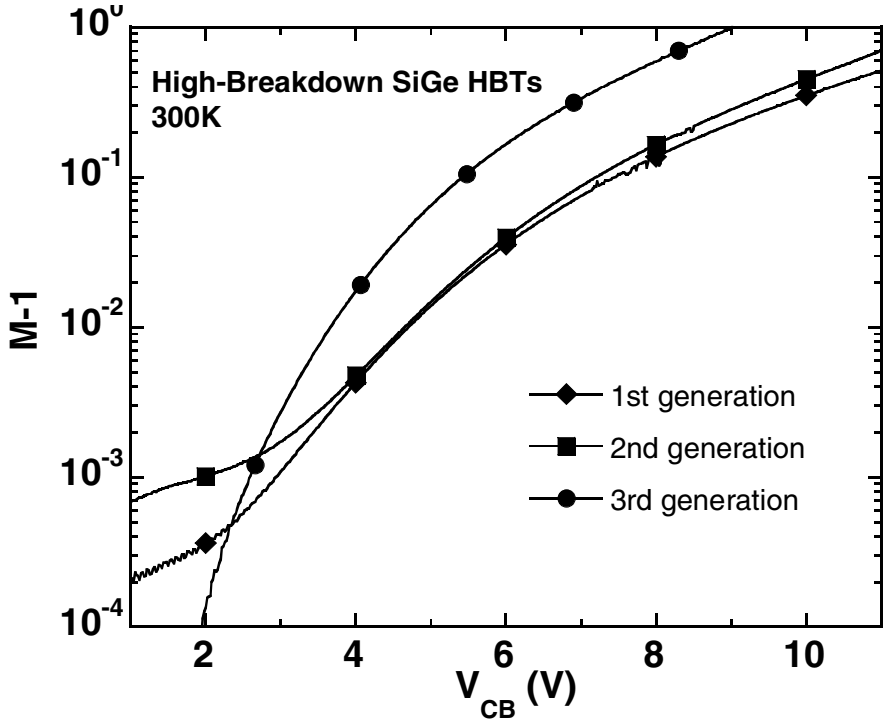

Figure 19: $M - 1$ characteristics for HB devices from three generations of SiGe HBT technology.

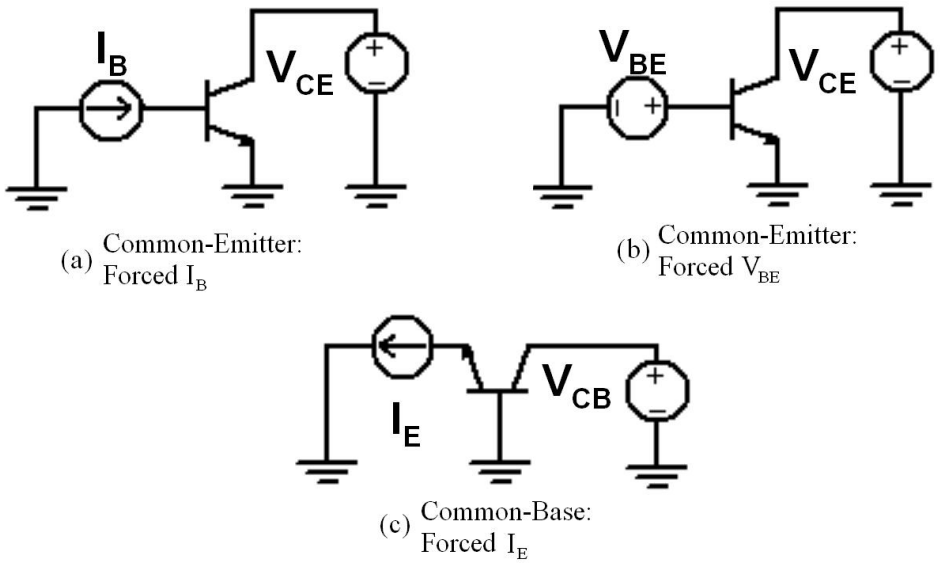

Figure 20: Common-emitter (forced I_B and forced V_{BE}) and common-base *dc* bias configurations.

Operational voltage limits were experimentally characterized for SiGe HBTs in both common-emitter (CE) and common-base (CB) operating configurations. The three different bias configurations compared in this study are shown in Figure 20. Each configuration shows avalanche breakdown behaviors that are distinct unto itself as described in the following sections.

3.2.2 Common-Emitter Bias with Forced Base Current

For the common-emitter bias configuration driven by a constant base current (CE-I_B), the base current is held constant by an external current source. This case is functionally similar to open-base configuration, except here I_B is non-zero. As a result, excess holes that are generated by impact ionization in the collector base depletion region are injected into the emitter [32]. Thus, the injected avalanche current is amplified by the forward current gain β across the emitter-base junction, which increases the collector current and avalanche current. This positive feedback leads to premature breakdown when the product $\beta(M-1)$ equals unity, as in the open-base case (BV_{CEO}). Therefore, increasing either β or $M-1$ will lead to a lower CE-I_B breakdown voltage. Overall, the CE-I_B configuration represents the worst-case in terms of operating voltage constraints, with breakdown occurring at voltages considerably lower than BV_{CBO}.

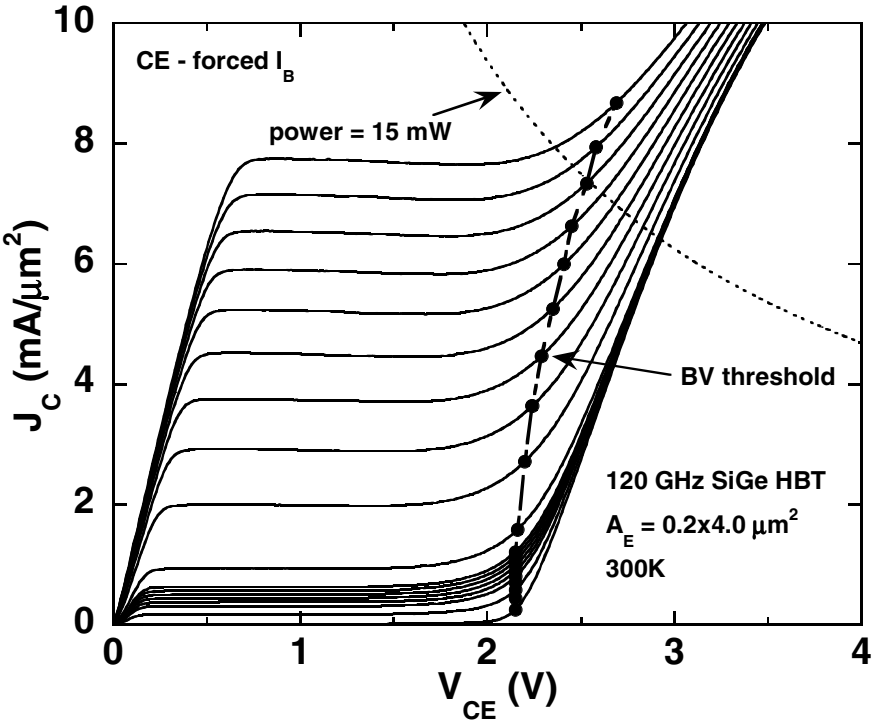

Figure 21: CE - forced I_B output characteristic with BV threshold indicated.

Figure 21 shows the CE-I_B output characteristics for a typical 120 GHz SiGe HBT. The breakdown voltage threshold is shown across bias [20]. Here this threshold increases with J_C because of three primary influences: the voltage drop across the parasitic collector resistance at high current (which reduces the internal collector-base reverse junction potential), decrease of β across bias, and reduction of $M - 1$ because of self-heating effects. Figure 22 shows measured CE-I_B operating voltage limits across bias (normalized to J_C at peak f_T) for the standard-performance SiGe HBTs from the three different technologies in Table 2. The role of an external series resistance (R_B) at the base is depicted for the 50 GHz SiGe HBT, showing the increase in the operating voltage limit across bias as the R_B is reduced from infinity (I_B drive) to zero (V_{BE} drive). Similarly, Figure 23 shows the measured CE-I_B breakdown limits for the high-breakdown devices across the three technology generations. A strong compression of the breakdown voltage limit is observed with technology scaling as a result of increases in $M - 1$ and β. The HB devices show a decrease in the CE-I_B BV threshold as current increases. Compared to the HS devices, this difference is primarily attributed to the fact that the HB devices operate at considerably lower collector current, which results in less parasitic voltage drop in the collector region.

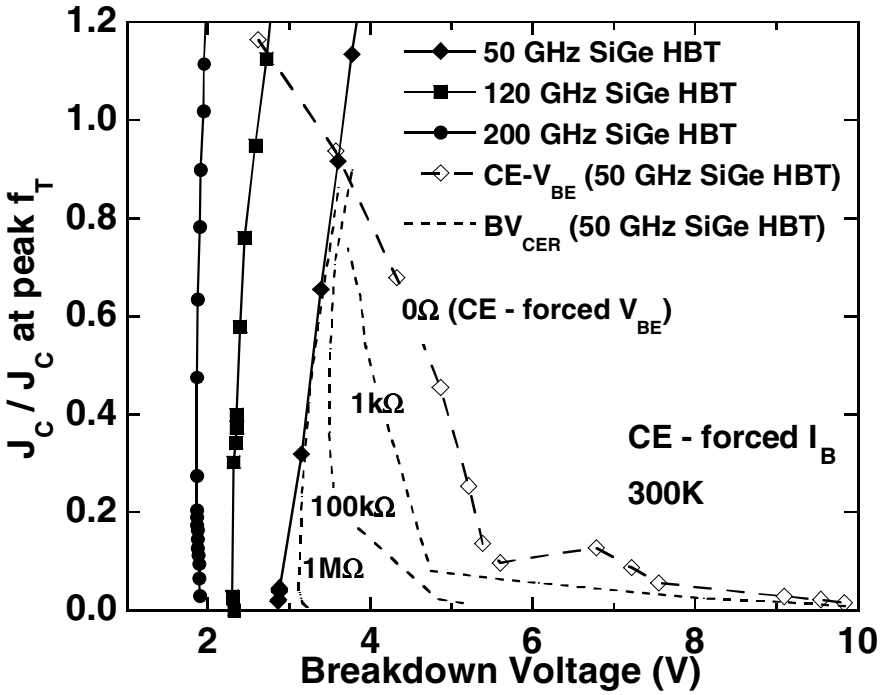

Figure 22: CE - forced I_B BV thresholds for HS devices from three generations of SiGe HBT technology. An external resistance on the base terminal is varied between 0 Ω (CE operation with fixed V_{BE} drive) and 1 M Ω for the 50 GHz peak f_T device.

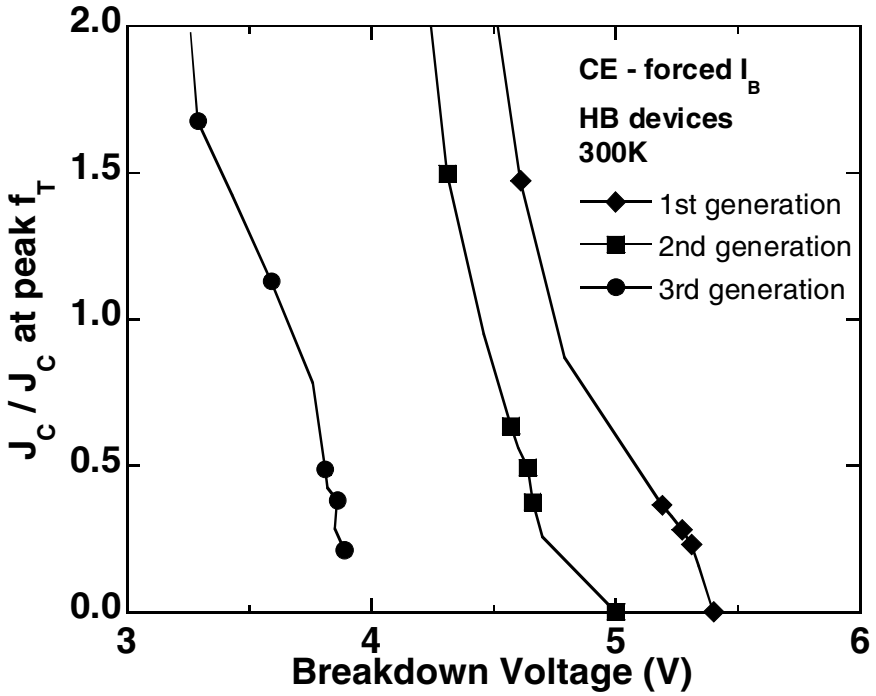

Figure 23: CE - forced I_B BV threshold for HB devices from three generations of SiGe HBT technology.

3.2.3 Common-Emitter Bias with Forced Base Voltage

For practical circuits, the base terminal of the SiGe HBT is not typically driven by a high-impedance (e.g. *current*) source as would be used for CE-I_B operation. Therefore, a second operating configuration of interest is the common-emitter bias driven by a constant base-emitter voltage (CE-V_{BE}), which is more commonly encountered in practical circuits.

The forced-V_{BE} driving condition differs from the forced-I_B case because the low external impedance to ground at the base allows excess hole current (generated by impact ionization) to exit the base terminal. At sufficiently high collector voltage (approximately BV_{CEO}) the product of the current gain and the avalanche multiplication factor exceeds unity and the base current reverses sign. As discussed previously, this reversal of base current, with increased V_{CB}, can eventually lead to central current crowding and bias instabilities. However, depending on the circuit application, stable bias can still be achieved (and may in fact be required) in regions of considerable base current reversal; thus, CE-V_{BE} bias allows operation at higher voltages (between BV_{CEO} and BV_{CBO}) than does CE-I_B bias [2], [34]. This is demonstrated in Figure 24, which shows the CE-V_{BE} output characteristics and voltage operating limits across bias for the same transistor measured in Figure 21. The CE-V_{BE} breakdown voltage constraints are influenced by a complicated set of electro-thermal interactions [3], [32] - [36]. The combined role of pinch-in and self-heating effects in the CE-V_{BE} configuration produces a complex dependence for the operating voltage limits across bias, and considerable differences in behavior are observed as V_{BE} (I_C) increases.

For low V_{BE} the device can sustain collector voltages considerably higher than BV_{CEO}, but eventually undergoes electro-thermal runaway at high V_{CE}. This instability occurs when self-heating causes a sufficient increase in the base-emitter junction temperature. As a result the emitter and collector currents will increase and act as positive feedback to further heat the device. This will result in a fly-back characteristic of the collector current, as shown in Figure 25, which presents a bistability condition for fixed V_{BE} operation and represents its maximum voltage limit [37]. As the collector voltage is increased beyond this point, the device abruptly enters breakdown as I_C rapidly increases until either destroying the device or reaching an external limit. Pinch-in effects resulting from base-current reversal can aggravate or even serve as a trigger for the CE-V_{BE} instability [34].

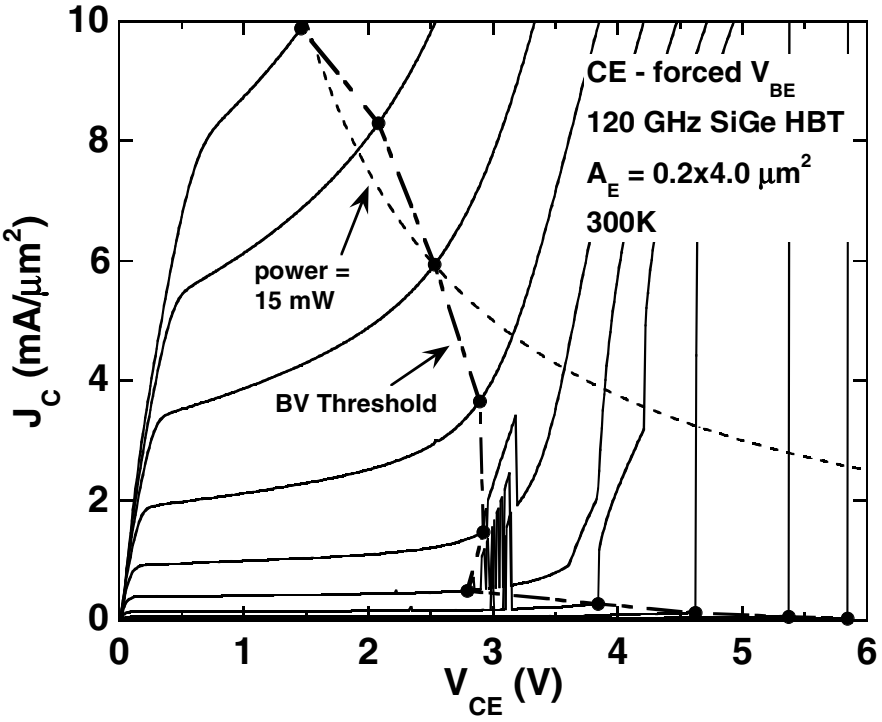

Figure 24: Common-emitter output characteristics at constant V_{BE} (CE-V_{BE}) with associated BV threshold.

However, Figure 25 shows that these bistable conditions are not present at high V_{BE}. In this region the CE-V_{BE} voltage limit is determined primarily by self-heating, which causes the collector current to increase in a stable manner with V_{CE}. Under high current conditions, base current reversal will be limited by of self-heating effects, which reduce $M - 1$ and increase the forward injected base current component. Figure 26 shows that for higher V_{BE}, $|I_{B\_rvs}|$ reaches a peak and then begins to decrease as V_{CE} increases. As a result, pinch-in effects do not play a role under high injection conditions. The transition between the low-current operating limits (dominated by fly-back instabilities and pinch-in effects) and the high-current operating limits (dominated by self-heating effects) is indicated by the bend in the BV threshold across bias.

The HS and HB CE-V_{BE} breakdown voltage limits are shown across bias in Figures 27 and 28, respectively. These results show that the fixed-V_{BE} voltage limits vary with bias to a much greater extent than the fixed-I_B voltage limits. The voltage limit is highest at very low currents, where it approaches BV_{CBO} but decreases rapidly as current increases because of pinch-in effects. Figure 27 shows that self-heating effects play a stronger role in the high-current voltage limits of first- and second-generation SiGe HBTs compared to those of the third-generation device.

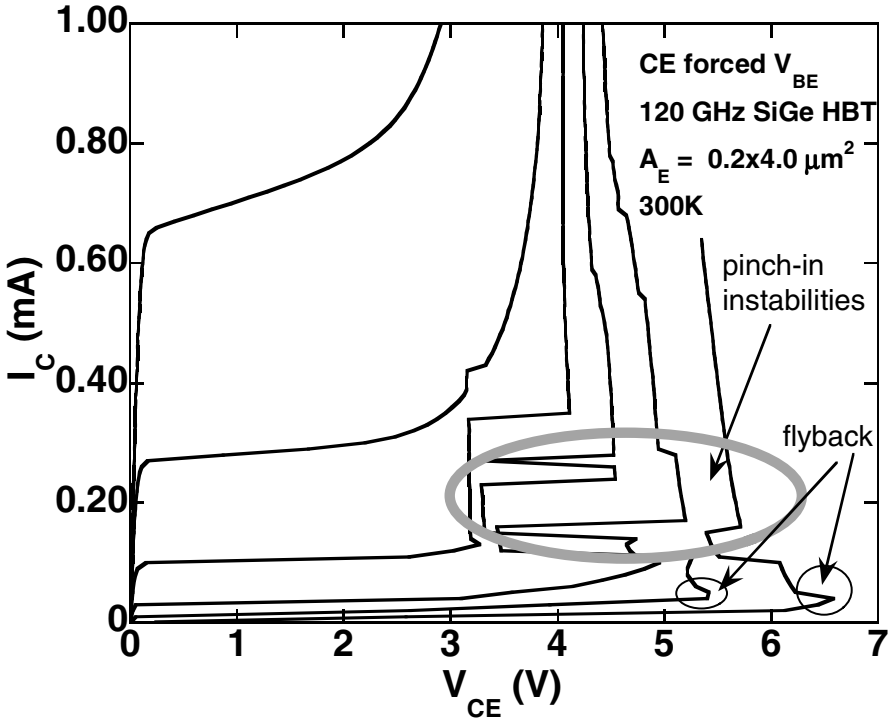

Figure 25: CE - forced V_{BE} output characteristic with I_C swept and V_{CE} measured.

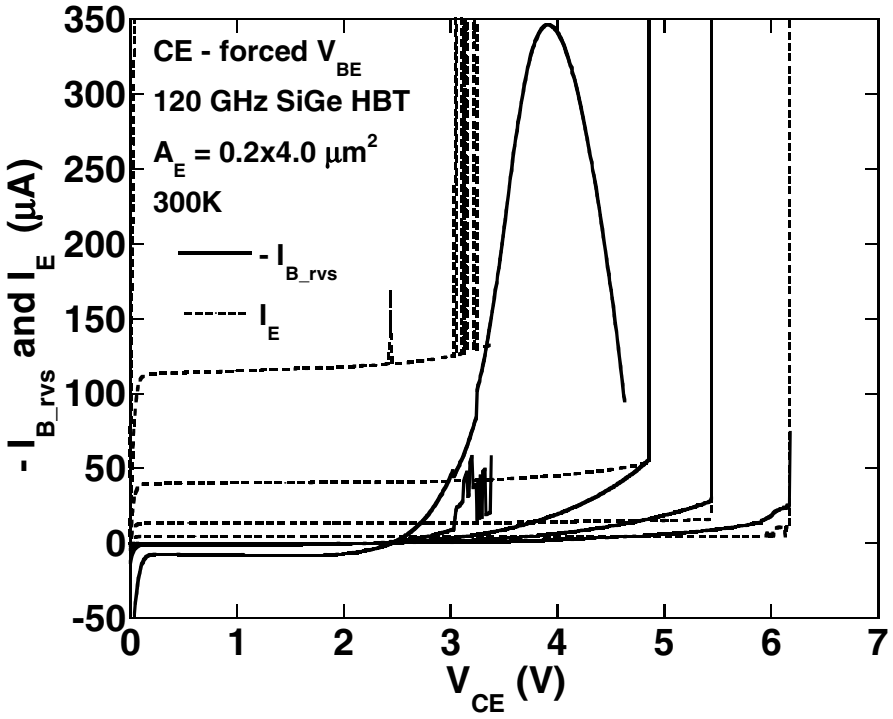

Figure 26: Reverse base current and emitter current characteristics resulting from CE - forced V_{BE} measurement.

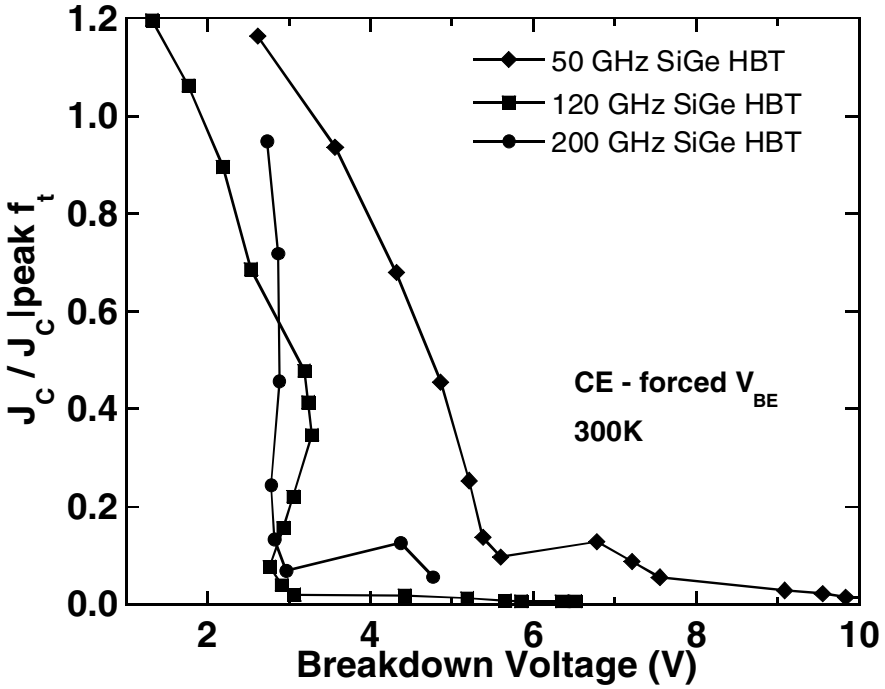

Figure 27: CE - forced V_{BE} BV thresholds for Hs devices from three generations of SiGe HBT technology.

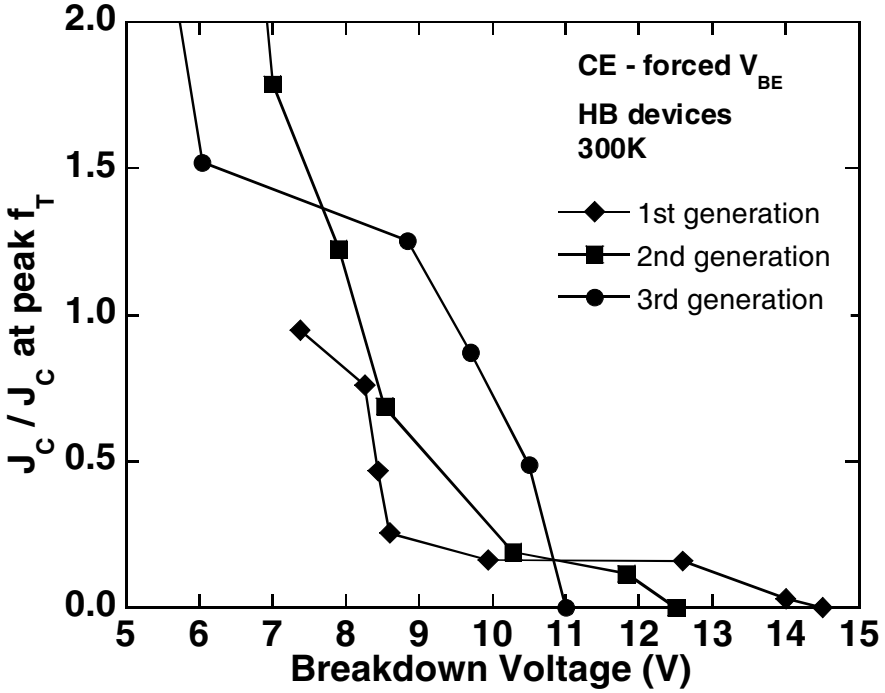

Figure 28: CE - forced V_{BE} BV threshold for HB devices from three generations of SiGe HBT technology.

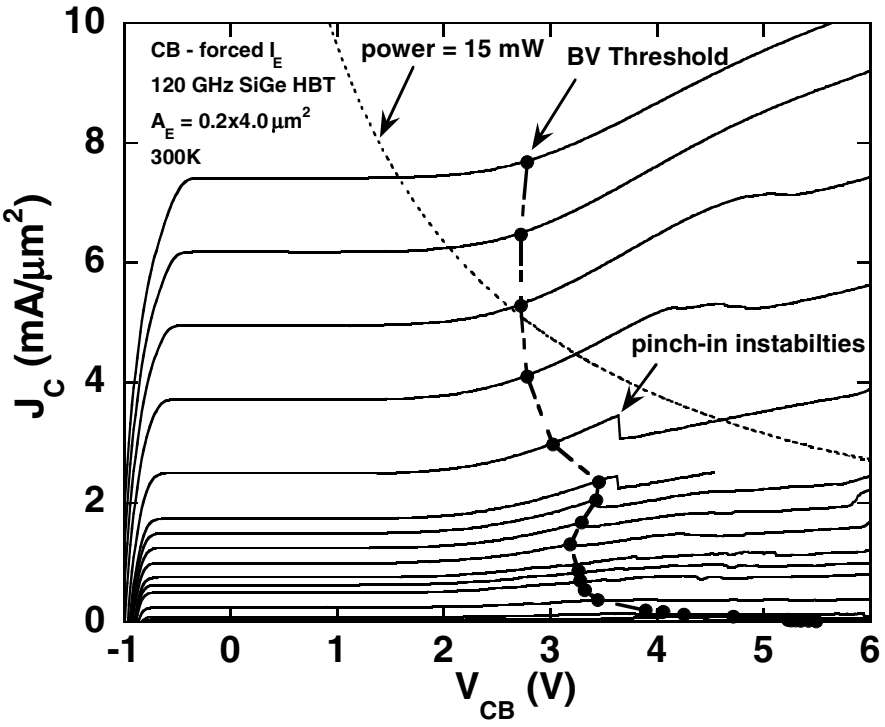

Figure 29: CB - forced I_E output characteristic with associated BV threshold.

3.2.4 Common-Base Bias with Forced Emitter Current

The common-base bias configuration driven by a constant emitter current (CB-I_E) lends itself to many practical circuit topologies, such as cascode stages, output buffers, and differential pairs. Like CE-V_{BE}, the CB-I_E driving condition allows excess hole current resulting from impact ionization to exit the base terminal, which can lead to central current crowding and pinch-in instabilities at high V_{CB}. However, since stable bias is possible under conditions of considerable base current reversal, the CB-I_E bias allows operation at higher voltages (between BV_{CEO} and BV_{CBO}) than does CE-I_B bias [2]. Moreover, since the I_E is held constant, electro-thermal runaway, as may occur in the case where V_{BE} is held constant, is prevented during CB-I_E operation as long as $V_{CB} < BV_{CBO}$. Figure 29 shows typical CB-I_E output characteristics for a second-generation SiGe HBT, with the BV threshold indicated across bias. Similar to CE-V_{BE} operation, this voltage limit is primarily determined by pinch-in effects at low-injection and by self-heating effects at high-injection [20].

Figure 30 shows V_{BE} and I_B measured at the device terminals for the SiGe HBT during CB-I_E operation. At high current the V_{BE} will decrease as a function of V_{CB} because of self-heating effects and the voltage drop of the reverse base current across the parasitic base resistance [2], [20], [34].

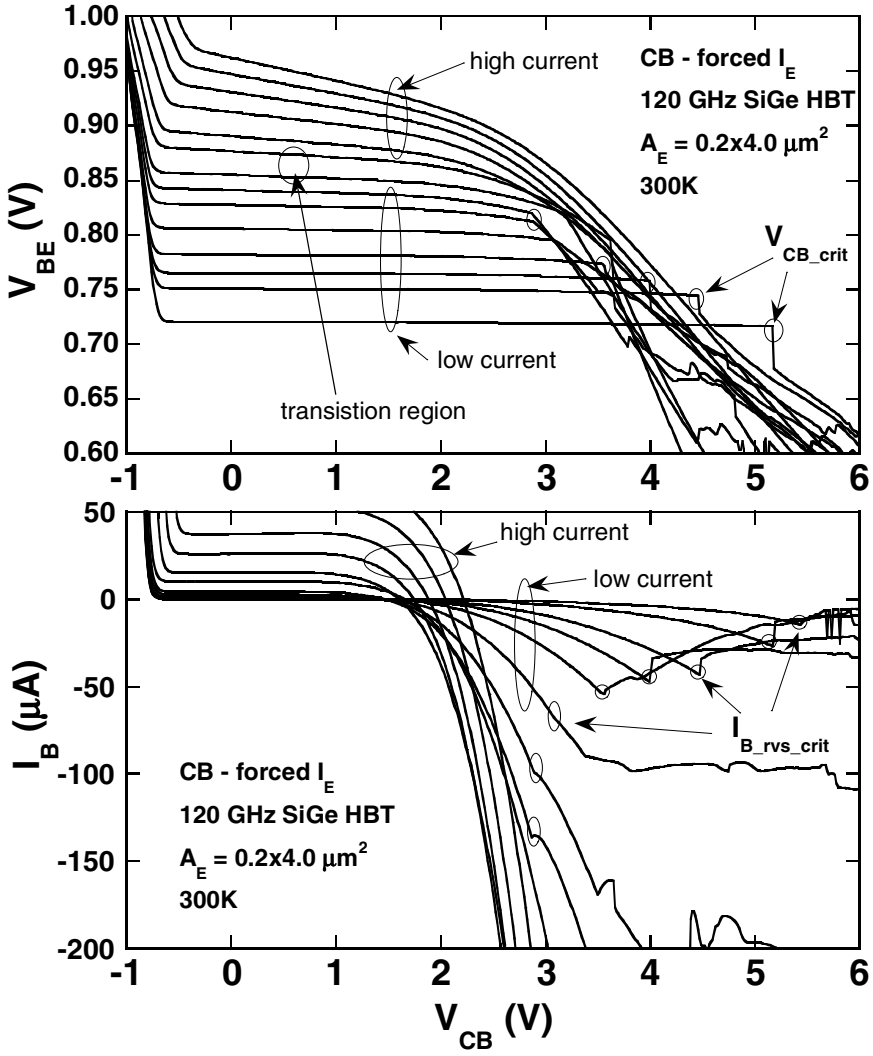

Figure 30: V_{BE} and I_B characteristics from CB - forced I_E measurements at low- and high-injection.

Pinch-in effects are observed at low current, as indicated by the discontinuities that occur at high V_{CB} in both the V_{BE} and I_B characteristics. The "critical" collector voltage $V_{CB-crit}$ is defined as the voltage where pinch-in occurs. Figure 30 also shows that the reverse base current at the pinch-in point ($I_{B\_rvs\_crit}$) can vary considerably over bias. This results in a strong bias dependence of the CB-I_E voltage limit, which approaches BV_{CBO} as I_E approaches zero. The bias-dependence of common-base pinch-in effects are examined analytically and experimentally in the next section.

The HS and HB CB-I_E breakdown voltage limits are shown across bias for three different SiGe HBT technology generations in Figures 31 and 32, respectively. These results show that, compared to the other bias configurations, the CB-I_E configuration can provide larger maximum operating voltage across bias. Despite increasing $M - 1$ with technology scaling, the third-generation SiGe

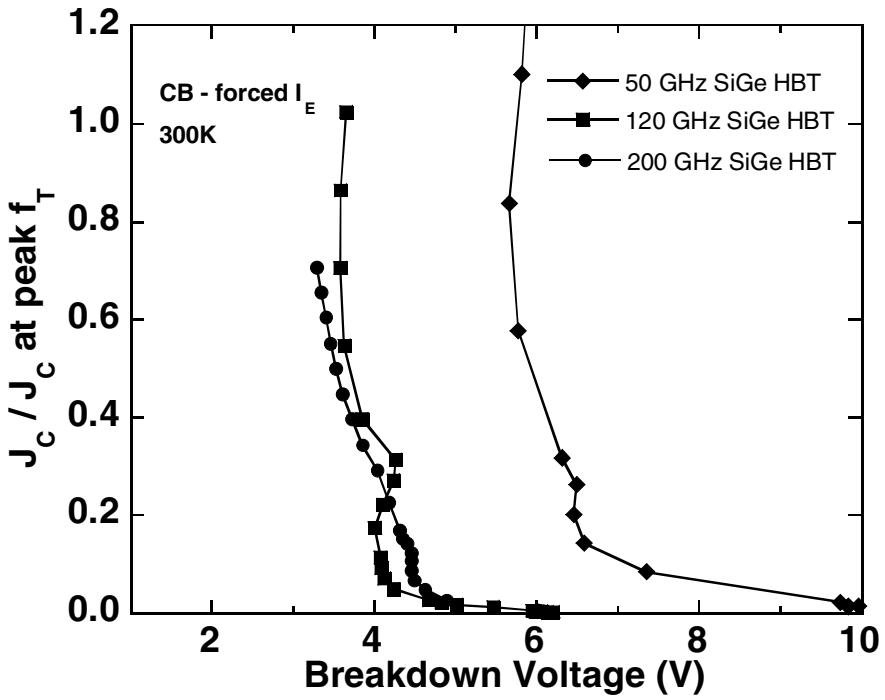

Figure 31: CB - forced I_E BV threshold for HS devices from three generations of SiGe HBT technology.

HBT does not show a significant reduction in the CB voltage limit. This observation is attributed to lateral scaling optimizations that reduce the parasitic base resistance, which strongly influences pinch-in, and is explored further in Section 3.3.

3.2.5 Summary

This comprehensive study of breakdown voltage in state-of-the-art SiGe HBTs presents a broad range of experimental results that document the role of device configuration, bias, collector design, and technology generation on the device operating voltage limits. Trans-generational device scaling for increased peak f_T performance in SiGe HBTs is accompanied by compression of their operational voltage limits, which represents an important concern for large-signal dynamic range and reliability in high-frequency transceivers. However, lateral scaling optimizations, which reduce the parasitic base resistance between the second- and third-generations, serves to offset this trend with respect to pinch-in effects [2]. Moreover, these trends (as reflected in Figure 2) show an overall increase in the combined product of breakdown voltage and peak f_T, an important figure-of-merit

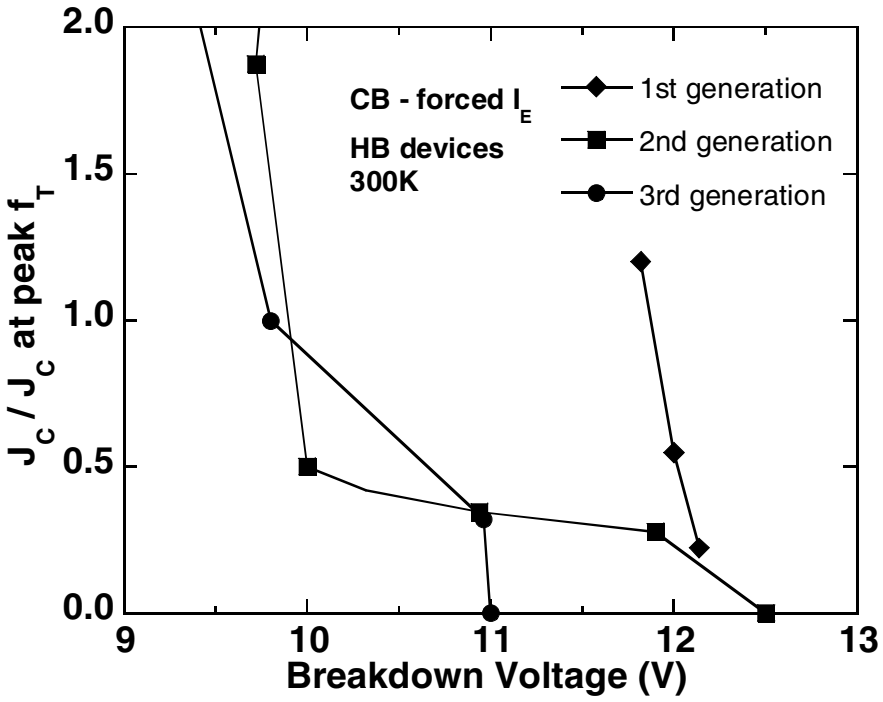

Figure 32: CB - forced I_E BV threshold for HB devices from three generations of SiGe HBT technology.

to gauge the trade-off between device speed and ruggedness. Therefore, despite the compression of operating voltage limits, the continued improvement in the $BV \cdot f_T$ product is good news for technology scaling in SiGe HBTs.

Overall, these results also show that the CB-I_E bias configuration allows a substantially higher maximum collector voltage than does the CE-I_B for all three SiGe HBT generations. The strong dependence of the CB operating voltage limit on bias current is also apparent. At high-injection CE-V_{BE} and CB-I_E voltage limits diverge considerably from one another as self-heating effects begin to strongly influence the *dc* behavior of the CE-V_{BE} configuration and degrade its high-current voltage operating limit. However, at low-injection the CE-V_{BE} and CB-I_E voltage limits are both primarily driven by pinch-in effects, and are therefore strikingly similar to one another in this region. Various factors that contribute to the bias dependence CB avalanche instabilities and pinch-in effects for SiGe HBTs will be addressed analytically and experimentally in the next section.

3.3 Analysis of Avalanche Instabilities in Advanced SiGe HBTs

3.3.1 Common-Base Breakdown Overview

Common-base (CB) operating voltage limits are of particular interest for several reasons. This configuration is useful in numerous practical circuit topologies, including cascode stages, output buffers, and differential pairs. In addition, it is well-known that CB operation can facilitate collector voltage bias above BV_{CEO}, making it useful for higher power applications that require a large output voltage swing.

This section discusses key device-level factors that contribute to the bias-dependent features observed in common-base (CB) *dc* instability characteristics of advanced SiGe HBTs. Parameters relevant to CB avalanche instabilities are identified, extracted from measured data, and carefully analyzed to yield improved physical insight, a straightforward estimation methodology, and a practical approach to quantify and compare CB avalanche instabilities.

For the CB bias configuration driven by a constant emitter current (or CB-I_E), the base current is not fixed by an external high-impedance *dc* source. As a result, excess hole current generated by impact ionization is allowed to exit the base terminal. At $V_{CE} \approx BV_{CEO}$ the product of the current gain (β) and avalanche multiplication factor ($M-1$) exceeds unity and I_B reverses sign, becoming negative [3], [32]–[36]. The voltage drop of the reverse base current across the distributed base resistance tends to increase the intrinsic E-B junction potential at the center of the device and acts as a positive feedback loop. Conversely, the voltage drop of I_E across the parasitic emitter resistance contributes negative feedback and reduces the intrinsic E-B junction potential at the center of the device. Overall, the potential distribution within the intrinsic base can result in the abrupt onset of central current crowding and bias instabilities at higher V_{CB} between BV_{CEO} and BV_{CBO} [13], [34]. These instabilities, often referred to as "pinch-in" effects, dictate to a large degree the maximum voltage limits for safe device operation in practical circuits [20].

Figure 33 shows the I_C and V_{BE} characteristics for a typical SiGe HBT in CB-I_E operation. At low V_{CB}, the emitter-base voltage decreases slightly because of the Early effect, and an increase in I_C is evident as the impact-ionization rate increases with V_{CB}. As base-current reversal (BCR) increases with V_{CB}, a discontinuity appears in the I_C and V_{BE} characteristics, indicating that the device has made a transition from 'normal' uniform operation to 'pinched' operation, for which the

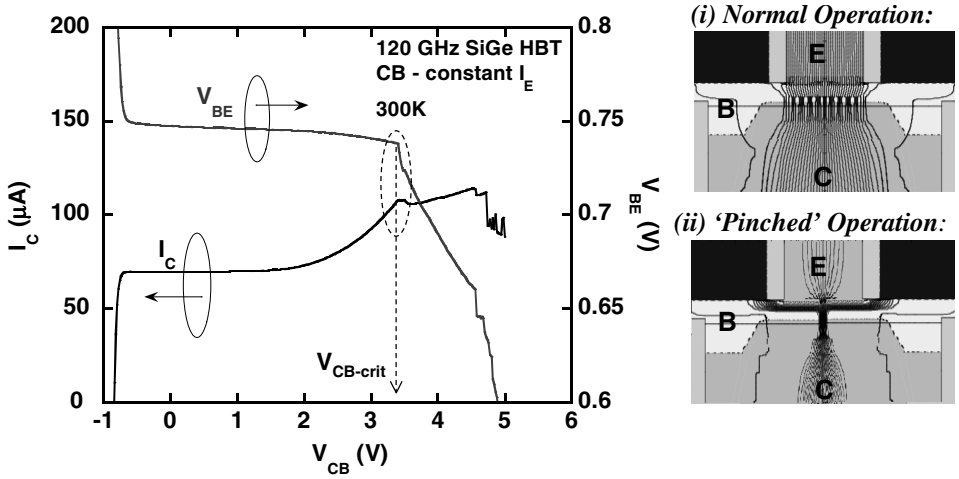

Figure 33: Typical I_C (left axis) and V_{BE} (right axis) characteristics CB - forced I_E operation. The collector voltage instability threshold $V_{CB-crit}$ is indicated. The adjacent graphic illustrates current density flowlines superimposed on a 2D SiGe HBT device cross section for (i) "Normal" operation ($V_{CB} < V_{CB-crit}$) and (ii) "Pinched" operation ($V_{CB} > V_{CB-crit}$).

majority of the current is constricted to a small region at the center of the SiGe HBT. The point where this transition occurs is defined as the "critical voltage" $V_{CB-crit}$. Instabilities that occur as a result of pinch-in are undesirable for device biasing and operation because they can result in inaccuracies in compact model simulations and can impact device or circuit reliability [20], [38]. Therefore, $V_{CB-crit}$ represents a prudent upper limit for collector voltage bias during CB-I_E operation.

$V_{CB-crit}$ can vary considerably as a function of current because of the respective positive and negative feedback influences associated with pinch-in. Thus, the bias dependence can be appear quite complex under close inspection, containing features not predicted by the conventional theory. For example, Figure 34 shows curves for I_C and I_B, measured on a second-generation SiGe HBT, with $V_{CB-crit}$ indicated across bias. A discontinuity in the $V_{CB-crit}$ characteristic is apparent at 3.4 V, and a minima in $V_{CB-crit}$ is observed at approximately 2.6 V. Based on these features, three distinct regions with differing breakdown behavior are identified and discussed below.

3.3.1.1 Strong Pinch-in

At very low current (region *A* in Figure 34), $V_{CB-crit}$ is characterized by a well-defined pinch-in, as indicated by clear and sudden discontinuities in the terminal characteristics, and tends to decrease from BV_{CBO} as I_E increases. Thus, it can be inferred that $(M-1)_{crit}$, which is the avalanche multiplication factor at $V_{CB-crit}$, likewise decreases with increasing I_E drive. The magnitude of

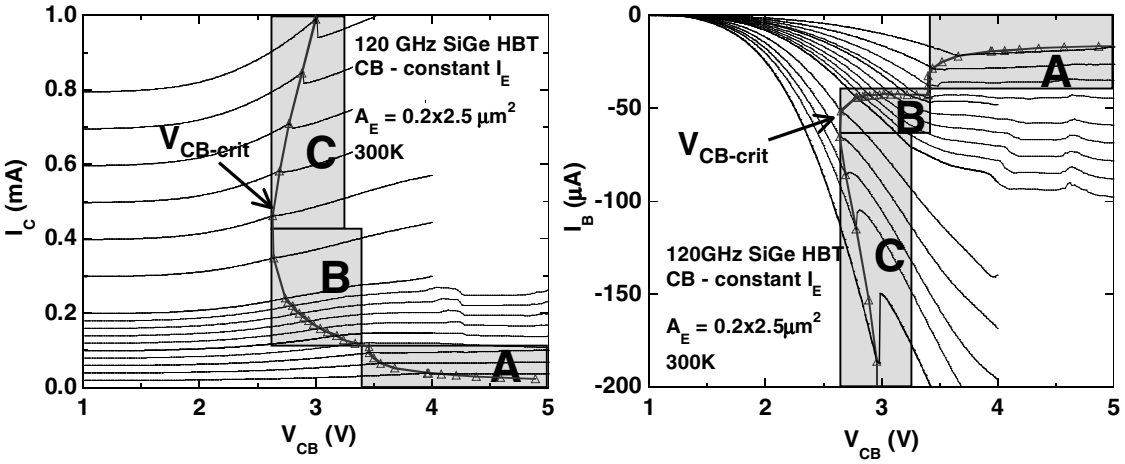

Figure 34: I_C (left graph) and I_B (right graph) from CB-I_E output characteristics with $V_{CB-crit}$ (triangles) indicated across bias. Three distinct CB-stability regions, which demonstrate different $V_{CB-crit}$ behavior across bias, are highlighted: *Region 'A'* - strong pinch; *Region 'B'* - weak quasi-pinch; *Region 'C'* - strong quasi-pinch.

the critical reverse base current ($I_{B-rvs-crit}$) increases with I_E in a near-linear fashion because of the ballasting effect of the parasitic emitter resistance r'_e. As a result, $V_{CB-crit}$ approaches a constant value at the upper bound of the strong pinch region. With the onset of strong pinch-in at $V_{CB-crit}$, the rate that the effective base resistance r'_b increases with respect to V_{CB} is much greater than that of r'_e, so that a high degree of pinch-in is rapidly achieved. Here the statistical die-to-die variation of $V_{CB-crit}$ is very small (standard deviation of less than 50 mV, or 2%), indicating highly predictable pinch-in behaviour. Strong-pinch conditions have been shown to affect mixed-mode reliability degradation, because hot carriers generated during pinch-in are further displaced from the E-B spacer region and thus have lower energy and cause less damage at the oxide interface [39].

3.3.1.2 Weak Quasi-Pinch-in

With increased current (region B in Figure 34), $V_{CB-crit}$ becomes less well-defined, undergoing either "soft" pinch-in that lacks clear discontinuities in the terminal characteristics, or random fluctuations between "pinched" and "stable" states. This region represents a balancing of the operative positive and negative feedback mechanisms, implying that r'_b and r'_e increase with V_{CB} at an approximately equal rate to one another. As a result, neither influence is dominant to clearly determine the threshold of device stability. Therefore, a prolonged state of partial current collapse is achieved

with respect to V_{CB}, mitigating the negative feedback effect of r'_e. Consequently, the conditions for quasi-instability are less rigorous compared to strong pinch-in and occur at lower V_{CB}, resulting in an apparent branch in the $V_{CB-crit}$ characteristic . In this region $|I_{B-rvs-crit}|$ is near-constant across I_E and both $(M-1)_{crit}$ and $V_{CB-crit}$ decrease as I_E increases. Because the conditions for breakdown are defined vaguely here, they are more prone to random fluctuations, and hence are less predictable. Thus, die-to-die variation in $V_{CB-crit}$ is larger in this region (standard deviation up to 200 mV, or 7%). Also, mixed-mode damage during quasi-pinch conditions is expected to be more severe than for strong pinch-in, since the generation of hot avalanche carriers is less confined to the center of the device.

3.3.1.3 Strong Quasi-Pinch-in

As I_E is increased further (region *C* in Figure 34) the quasi-pinch-in branch begins to exhibit strong pinch-in characteristics and $V_{CB-crit}$ is once again well-defined. $|I_{B-rvs-crit}|$ increases with increasing bias and regains a near-linear relationship with respect to I_E, and $(M-1)_{crit}$ approaches a constant value. On certain devices, a successive swapping between strong quasi- and weak quasi-pinch regions has been observed across bias. As self-heating and high injection effects become more prominent at higher currents, $(M-1)$ for a given V_{CB} is decreased because of phonon scattering and a reduction of the peak E-field in the collector-base space-charge region (CB-SCR). As a result, $V_{CB-crit}$ tends to increase with I_E at higher currents.

3.3.2 General Relations and Analysis

3.3.2.1 Theory

Table I lists relevant parameters used in the analysis of CB stability. To examine $V_{CB-crit}$ as a function of bias in CB-I_E operation, the following relation, as introduced in [34] and further explored in [20], is applied:

$$|I_{B-rvs-crit}| = \frac{(v_o + r'_e \cdot I_E)}{r'_b}. \tag{36}$$

If the product $(M-1)\cdot\beta >> 1$, as can be assumed in the case of strong BCR, a simple ratio approximation for $M-1$ can be applied to Equation 36 to obtain an expression for the avalanche

Table 4: Important parameters used in the study of CB stability. Common parameters for normal device operation are listen in the first column. The second column shows the corresponding factors as defined at the onset of pinch-in when $V_{CB} = V_{CB-crit}$.

Parameter	$@V_{CB} = V_{CB-crit}$	Description
r_e (Ω)	r'_e	Effective emitter resistance resulting from current distribution nonuniformities
r_b (Ω)	r'_b	Effective base resistance resulting from current distribution nonuniformities
$(M-1)$	$(M-1)_{crit}$	Avalanche multiplication factor
I_{B-rvs} (A)	$I_{B-rvs-crit}$	Base current under conditions of BCR
ΔV_B (V)	ΔV_{B-crit}	Excess intrinsic base potential resulting from avalanche carriers and base resistance
-	v_o (V)	Intrinsic trigger potential: ΔV_{B-crit} for $r'_e = 0$
-	r'_e/r'_b	Pinched-resistance ratio
-	v_o/r'_b	$I_{B-rvs-crit}$ for $r'_e = 0$

multiplication factor required to induce pinch-in [20]:

$$(M-1)_{crit} \approx \frac{|I_{B-rvs-crit}|}{I_E} = \frac{v_o \cdot I_E^{-1} + r'_e}{r'_b}. \tag{37}$$

The factor r'_b physically represents the destabilizing effect resulting from the distributed (extrinsic and intrinsic) base resistance during BCR. The factor r'_e represents the degree to which the emitter resistance ballasts the intrinsic E-B voltage distribution and prevents the accumulation of junction potential at the center of the device. The term v_o represents the critical offset to the intrinsic base voltage required to trigger a pinch-in event if r'_e is set to zero. Although typically small in value, the v_o term is important because it is responsible for the general bias dependence of $(M-1)_{crit}$ that is observed experimentally.

The product of $|I_{B-rvs}|$ and r'_b equals the increase in the average intrinsic base potential from BCR and is represented by the term ΔV_B. From Equation 36, when ΔV_B exceeds a critical value ΔV_{B-crit}, pinch-in will occur according the relation

$$\Delta V_{B-crit} = |I_{B-rvs-crit}| \cdot r'_b = v_o + r'_e \cdot I_E. \tag{38}$$

ΔV_B and ΔV_{B-crit} are useful since they can be obtained from V_{BE} across V_{CB} from a CB-I_E measurement [21]. The technique used is similar to the one described in [40].

Overall, these relations provide a straightforward description of the feedback influences that determine the bias dependence of $(M-1)_{crit}$. For example, in Figure 35 the avalanche instability

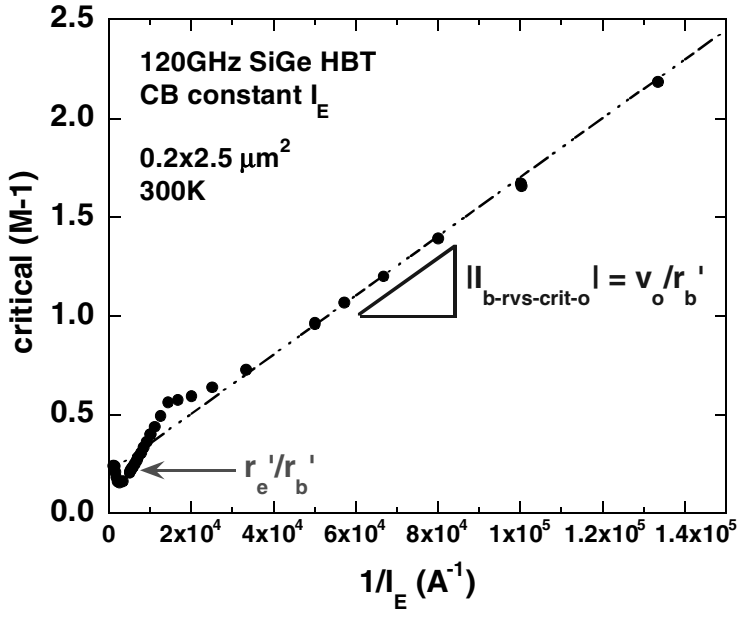

Figure 35: Measured and fitted $(M-1)_{crit}$ plotted as a function of $1/I_E$ (see Equation 37) for a 120 GHz SiGe HBT.

threshold $(M-1)_{crit}$ is extracted from the CB-I_E output characteristics for a second-generation (120 GHz) SiGe HBT and plotted as a function of $1/I_E$ to take the form of Equation 37. The bias dependence of $(M-1)_{crit}$ is depicted, showing a slope of v_o/r'_b with respect to $1/I_E$. This slope term is equal to $|I_{B-rvs-crit}|$ in the special case that either r'_e or I_E is set to zero. As such, this term describes the low-current sensitivity to pinch-in for the device, independent of emitter ballasting, and is referred to as the *avalanche trigger*. The y-intercept of Equation 37 shows that $(M-1)_{crit}$ will asymptotically approach the *pinched-resistance ratio* r'_e/r'_b at the high-current limit. Together, r'_e/r'_b and v_o/r'_b serve as simple and useful metrics for first-order modeling and comparison of CB avalanche instability characteristics over bias.

3.3.2.2 Influence of Strong and Weak Pinch-in

The implied assumption that both r'_e/r'_b and v_o/r'_b are independent of bias is not entirely valid. As shown in Figure 35, some variation of the actual characteristic from the ideal linear fit is typically observed, thus implying a bias-dependence in either r'_e/r'_b or v_o/r'_b (or both). Since v_o/r'_b has considerably smaller influence on $(M-1)_{crit}$ as I_E grows large, and is typically well-fit at low I_E, the simplifying approximation that v_o/r'_b is bias independent is considered reasonable. Thus, the

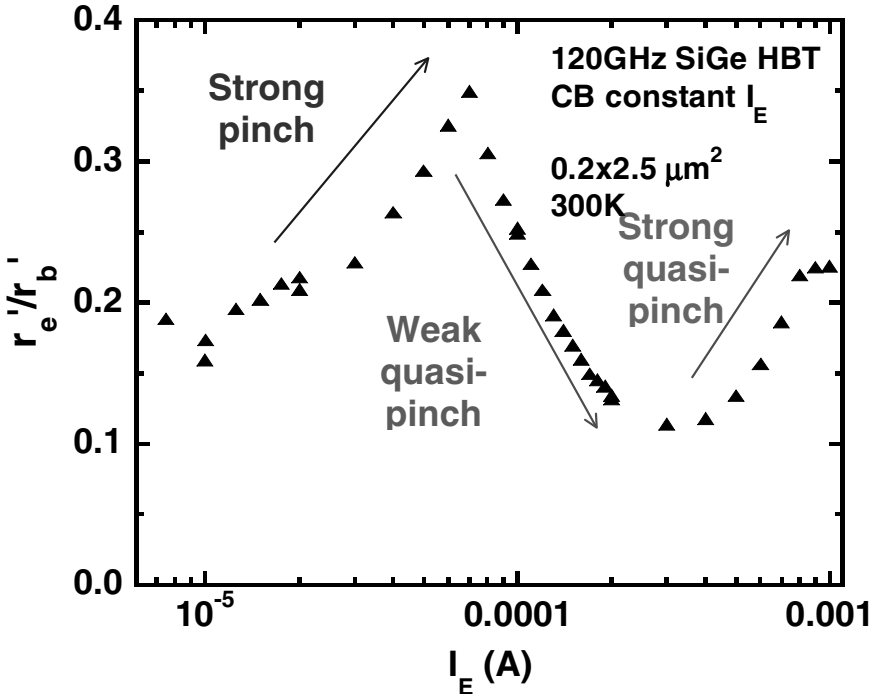

Figure 36: Extracted variation of r'_e/r'_b across bias due to the influence of the CB-stability regions: for strong pinch and strong quasi-pinch, r'_e/r'_b increases with I_E; for weak quasi-pinch, r'_e/r'_b decreases with I_E.

primary source of variation from the ideal fit can be modeled as a bias dependent variation of the pinched-resistance ratio for fixed v_o/r'_b.

From the discrepancy between the *actual* and *fitted* values for $(M-1)_{crit}$, as shown in Figure 35, the bias-dependent pinched-resistance ratio can be determined for any I_E with the following relation:

$$\left.\frac{r'_e}{r'_b}\right|_{I_E} = (M-1)_{crit}|_{I_E} - (M-1)_{crit-fitted}|_{I_E} + (r'_e/r'_b)_{fitted}, \tag{39}$$

or, from Equation 37,

$$\left.\frac{r'_e}{r'_b}\right|_{I_E} = \frac{I_{B-rvs-crit}(I_E) - v_o/r'_b}{I_E}. \tag{40}$$

This variation of the pinched-resistance ratio over bias, calculated using Equation 40, is shown in Figure 36 for a typical device. Close inspection shows that the nature of the r'_e/r'_b variation across bias is directly related to the CB stability regions discussed in Section 3.3.1. For instance, for strong pinch-in and strong-quasi pinch, r'_e/r'_b increases with I_E. This occurs because a higher degree of intrinsic base potential non-uniformity is required to overcome the ballasting effect of

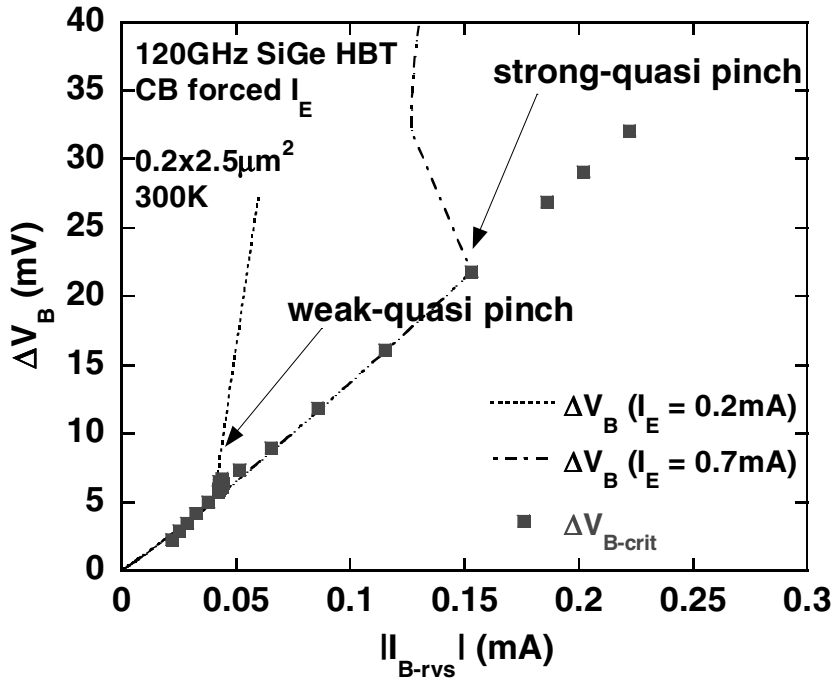

Figure 37: ΔV_B for $I_E = 0.2$ mA and $I_E = 0.7$ mA, and ΔV_{B-crit} across bias plotted as a function of $|I_{B-rvs}|$. The position where ΔV_B changes slope indicates pinch-in (ΔV_{B-crit}).

$r'_e \cdot I_E$ as I_E increases. This voltage nonuniformity translates into a current injection nonuniformity, which results in a higher effective emitter resistance. Eventually, the effective emitter resistance is large enough so that an equilibrium is established between r'_e and r'_b at the onset of pinch-in. As a result, abrupt current collapse is prevented and weak quasi-pinch-in occurs. The effective emitter resistance is lower under partial pinch conditions, and therefore r'_e/r'_b decreases with I_E in the weak quasi-pinch region.

The influence of the CB-stability regions is also observable with respect to ΔV_B, which is plotted in Figure 37 as a function of reverse base current for $I_E = 0.2$ mA and $I_E = 0.7$ mA. The point at which pinch-in occurs is indicated by an abrupt change in the slope of ΔV_B with respect to $|I_{B-rvs}|$. In the weak-quasi pinch region (e.g., $I_E = 0.2$ mA), this slope changes drastically due to increase in effective base resistance, yet remains positive. However, in the cases of strong pinch and strong-quasi pinch (e.g., $I_E = 0.7$ mA), the slope of ΔV_B becomes negative at instability threshold, resulting in a switchback characteristic because of the decrease in BCR caused by complete pinch-in.

From Equation 40 a straightforward estimate for the effective emitter and base resistances at pinch-in can be obtained. In this typical case for the device depicted in Figures 35, 36 and 37, r'_b shows a steady decrease of about 25% across the range of I_E. This trend is consistent with the decrease in the intrinsic base resistance due to base conductivity modulation at higher current levels [41]. However, r'_e is observed to vary in excess of +/- 40%, because of the influence of the CB-stability regions across bias.

3.3.3 Experimental Results

Commercially available second- and third-generation and experimental fourth-generation (300 GHz) SiGe HBTs with various emitter stripe sizes were measured to examine the role of device geometry and technology scaling on CB avalanche instabilities in state-of-the-art SiGe HBTs. All *dc* measurements were performed at room temperature using an Agilent 4155C Semiconductor Parameter Analyzer.

3.3.3.1 Analysis of Geometry Dependence

CB-I_E *dc* characteristics were measured across a wide range of bias (from J_C of 1 μA/μm^2 to 1 mA/μm^2) on second-generation (120 GHz) SiGe HBTs with various emitter stripe sizes in order to determine the role that device area plays on the CB stability parameters. The results from these measurements are summarized in Figure 38, which shows extracted r'_e/r'_b and v_o as a function of emitter length (L_E), for three different emitter stripe widths (W_E). Here v_o is observed to be on the order of 2 mV or less, upwards of 10x lower than given in [34], which derives v_o to be equal to the thermal voltage V_T (26 mV at 300 K). This shows that CB stability in practical SiGe HBTs is far more delicate than predicted by the simple theory, requiring a substantially smaller increase in intrinsic base voltage to trigger pinch-in.

As shown in Figure 38, increasing L_E from 2.5 μm to 10 μm causes v_o to decrease by about 1 mV, evidence of the importance of the emitter-length dimension in initiating pinch-in. At the same time, r'_e/r'_b increases from approximately 0.2 to 0.3. This implies that the reduction in r'_e with L_E is countered by a greater reduction in r'_b for a slight enhancement to device stability at a given I_E. Interestingly, these data show only small, non-monotonic variations of pinched-resistance ratio as a function of W_E, suggesting the important role that the extrinsic base resistance plays in pinch-in

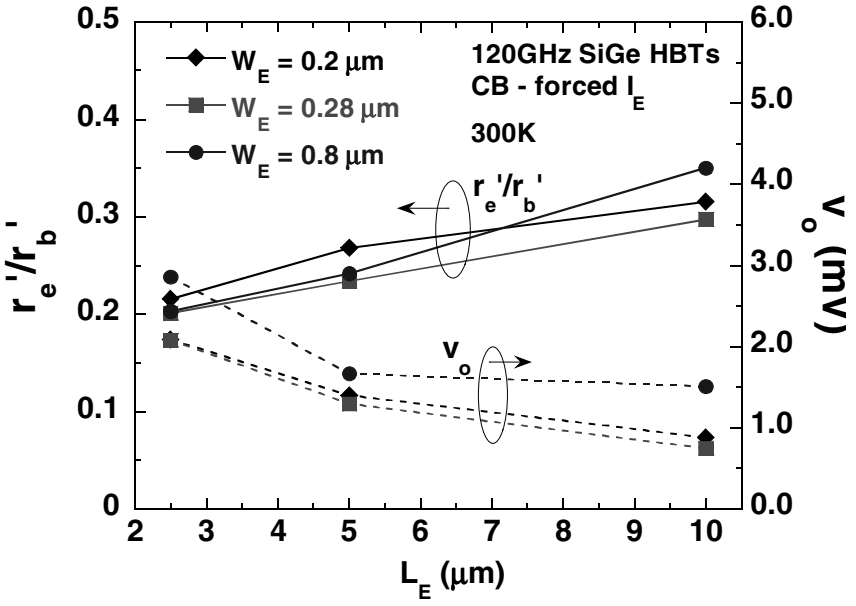

Figure 38: Extracted r'_e/r'_b and v_o for 120 GHz SiGe HBTs with various device sizes.

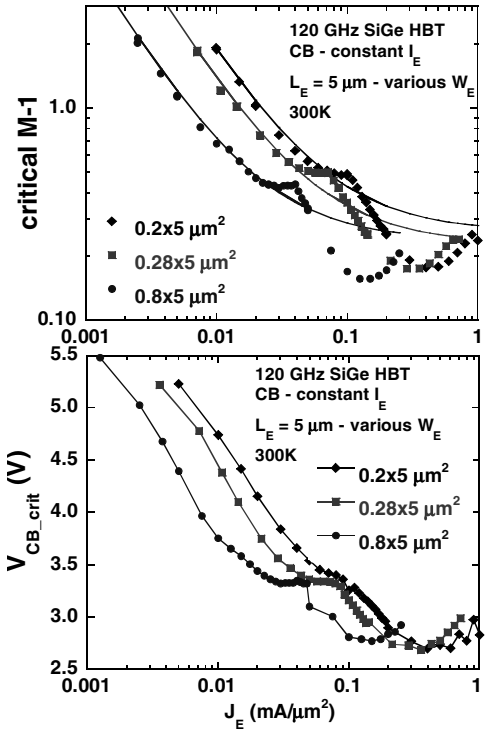

Figure 39: $(M-1)_{crit}$ (top graph) and $V_{CB-crit}$ (bottom graph) vs. J_E for various device geometries. For $(M-1)_{crit}$, fitted curves (solid lines) from extracted r'_e/r'_b and v_o parameters are compared with the measured data.

behavior for this second-generation device. In addition, these results show that the stability of the intrinsic base potential distribution is far more sensitive to variations in L_E than to W_E. Overall, it is clear from Figure 38 that these stability parameters do not scale directly with A_E, which is important to note when considering the role of $V_{CB-crit}$ across current *density.*

When the results from Figure 38 are used to generate fitted curves for $(M-1)_{crit}$ as a function of I_E (not shown), only a small overall variation is observed among the different device geometries. However, when viewed instead as a function of emitter current density (J_E), a pronounced geometrical dependence becomes apparent. Figure 39 shows both $(M-1)_{crit}$ and $V_{CB-crit}$ as a function of J_E for three emitter widths. For comparison, both the fitted and measured results for $(M-1)_{crit}$ are shown. In the strong pinch-in region at low current, these devices exhibit as much as 1 V reduction in $V_{CB-crit}$ for a fixed J_E as W_E increases from 2.5 μm to 10 μm. This geometry dependence is significant for circuit applications and is well-captured by the CB-stability parameters (r'_e/r'_b and v_o/r'_b), as indicated by fitted curves for $(M-1)_{crit}$. For an accurate approximation at higher current, the value and position of the minimum r'_e/r'_b should be noted as well.

3.3.3.2 Analysis of Layout Dependence

For this experiment CB-I_E *dc* characteristics were measured across a wide range of bias (from J_C of 1 μA/μm^2 to 1 mA/μm^2) on third-generation (200 GHz) SiGe HBTs with various transistor layout configurations, for several device geometries to investigate the role of device layout on CB stability parameters. The layouts compared include a single emitter stripe and a single contact for each terminal (*'CBE'*), a single emitter stripe flanked by two base contacts and two collector contacts (*'CBEBC'*), and two emitter stripes interleaved with three base contacts and flanked by two collector contacts (*'CBEBEBC'*).

Figure 40 shows $(M-1)_{crit}$ analysis for a typical third-generation SiGe HBT. In the weak quasi-pinch region the $(M-1)_{crit}$ characteristic shows a 'quasi-stable' behavior with two distinct CB stability thresholds for a single bias, indicating a particularly complex feedback relationship for pinch-in at the transition between strong pinch and weak quasi-pinch. This feature results in discontinuity in CB threshold characteristics and requires two different fitting curves to be accurately modeled across the entire range of bias. Thus, both a low-current fit and a high-current fit are

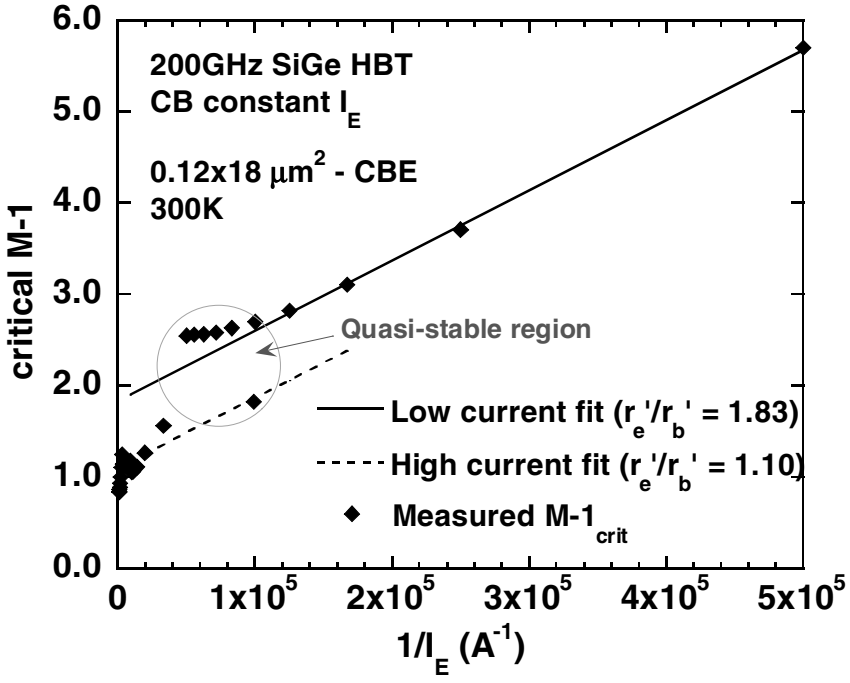

Figure 40: Measured and fitted $(M-1)_{crit}$ plotted as a function of $1/I_E$ (see Equation 37) for a 200 GHz SiGe HBT.

applied, each with a different y-intercept (r'_e/r'_b) values but both sharing the same slope (v_o/r'_b). Since the value obtained for the high-current fit is worst case and applies to the useful bias range for the device ($> 10\mu\text{A}/\mu\text{m}^2$), it represents a more practical parameter for comparison than the low current pinched-resistance ratio.

The results of the transistor layout study are summarized in Figure 41. Here, extracted parameters r'_e/r'_b (high-current value) and v_o plotted as a function of L_E for the three layout variations examined. The low-current stability term v_o shows a decreasing trend as the layout is varied from *CBE* to *CBEBC* to *CBEBEBC*. In addition, the decreasing trend across L_E for the third-generation SiGe HBT results in Figure 41 are similar to the results for second-generation SiGe HBTs shown in Figure 38. However, v_o is an order of magnitude lower in the third-generation SiGe HBTs, indicating that for a given r_b and at fixed $M-1$ this scaled technology node is more prone to pinch-in during low-current operation. However, the pinched-resistance ratio for the 200 GHz SiGe technology is considerably higher (around 4 to 5x) than for the 120 GHz SiGe technology due to parasitic base resistance optimization applied in the third-generation technology. Interestingly, only small

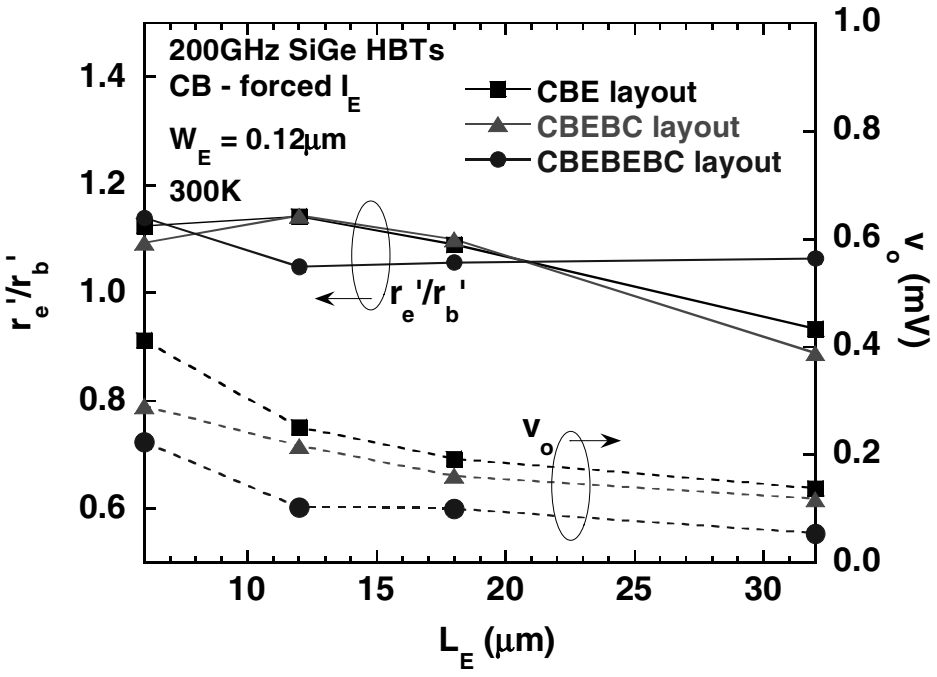

Figure 41: Extracted r'_e/r'_b and v_o for different device sizes and various layouts of 200 GHz SiGe HBTs.

differences for r'_e/r'_b are observed between layouts, although the two emitter finger layout shows less variation as L_E increases. This result suggests that a circuit designer may choose between these standard transistor layout configurations without drastically altering the CB-stability characteristics.

3.3.3.3 Analysis Using Two-Base Transistor Tetrode Structures

In this experiment, CB-I_E *dc* characteristics were measured on transistor tetrode structures fabricated in third-generation SiGe HBT technology. These unique devices have two base contacts and use an emitter ring to separate the two extrinsic base regions from one another [42]. Thus, these structures can be operated in standard bipolar transistor fashion, but the driving conditions of the two base terminals can be used to significantly alter the flow of base current and thus the parasitic base resistance properties of the tetrode structure during measurement. The purpose of this experiment is to examine and compare the CB stability threshold characteristics on these tetrode structures for standard (or symmetrical) operation and high-R_B (or asymmetrical) operation.

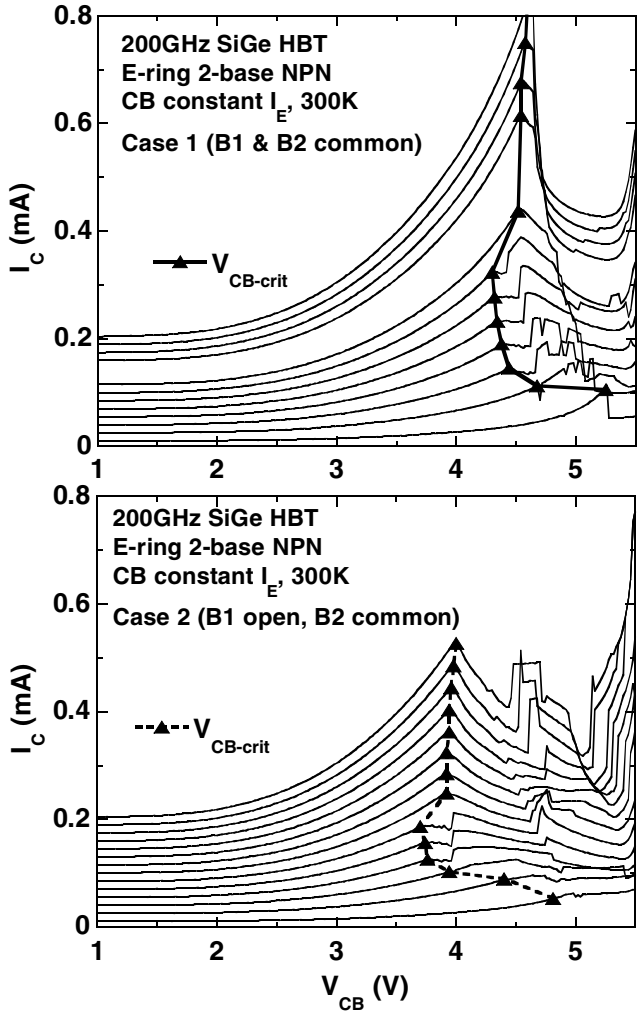

Figure 42: I_C vs. V_{CB} characteristics and CB stability thresholds measured on a double-base emitter-ring HBT structure in 200 GHz SiGe HBT technology. Two different driving conditions are compared.

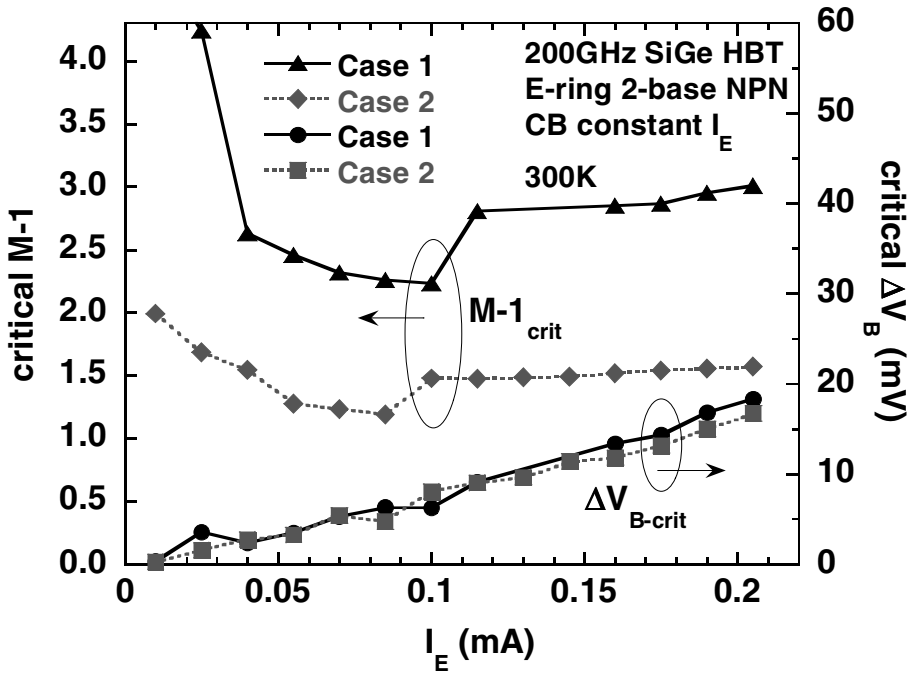

Figure 43: $(M-1)_{crit}$ and ΔV_{B-crit} vs. I_E measured on a double-base emitter-ring HBT structures in 200 GHz SiGe HBT technology. Two different driving conditions are compared. For 'Case 1' both base contacts are grounded. For 'Case 2' only one base contact is grounded while the other is open.

Figure 42 shows the I_C characteristics across V_{CB} for two driving conditions: 'Case 1' (standard operation), where both bases are grounded so that the parasitic extrinsic and intrinsic base resistances are minimized, and 'Case 2', where one base terminal is grounded while the other is open, which results in asymmetrical base current flow. This reduces the effective perimeter of the device and thereby increases base resistance. These results show $V_{CB-crit}$ is decreased by as much as 0.7 V (approximately 16%) during asymmetrical operation. This comparison illustrates that although typical layout variations examined in the previous experiment cause only minor changes to CB stability, layouts that significantly restrict the directional flow of avalanche generated carriers can significantly alter the pinch-in characteristics. Comparing these third-generation results with those in the previous section for standard device layouts shows the tetrode structures have significantly higher pinched-resistance ratio (ranging from 2.2 to 2.9, versus 1 to 1.1 for standard layouts) because of the higher perimeter-to-area ratio for these structures. This demonstrates the potential for unique opportunities to leverage transistor layout to increase CB stability in practical circuits.

For additional insight, $(M-1)_{crit}$ and ΔV_{B-crit} are plotted across bias in Figure 43. This result shows that $(M-1)_{crit}$ is reduced by almost a factor of two for Case 2, showing the effect of asymmetrical operation on the pinched-resistance ratio. However, ΔV_{B-crit} is similar between these two driving conditions, indicating that both cases require the about the same intrinsic base voltage offset to induce pinch-in. So, from Equation 38 it can be concluded that the stabilizing effect of r'_e is similar for both. But, because of higher r'_b during Case 2, ΔV_B increases more rapidly with I_{B-rvs}, causing pinch-in to occur at lower V_{CB}.

Additional measurements were taken on these tetrode structures in order to independently extract values for the parasitic emitter and base resistances using two different techniques [40], [43]. These results indicate that r'_b from Equation 38 is well-predicted by the extracted value for parasitic base resistance. However, r'_e tends to be on the order of 3x larger than the extracted emitter resistance, with considerable variation because of sensitivities to injected current distribution within the emitter.

3.3.4 Summary and Implications

Common-base avalanche instabilities in SiGe HBTs constitute an important operating limit for reliable device performance at high collector voltage (beyond BV_{CEO}), particularly as breakdown voltages continue to decrease with technology node scaling. Important CB-stability parameters are summarized in Table 5 for several SiGe HBT BiCMOS technology generations, including new results on fourth-generation (300 GHz f_T, 350 GHz f_{MAX}) SiGe HBTs. From this snapshot, curves approximating the critical $M-1$ (and thus $V_{CB-crit}$) can be reconstructed across bias to provide simple rule-of-thumb guidelines for device and circuit designers for usable maximum voltage bias under CB-I_E operation, as is shown in Figure 44.

These results show a drastic improvement in the pinched-resistance ratio between the second- and third-generation SiGe HBTs because of lateral scaling and optimizations to reduce base resistance. As a result, the third-generation SiGe HBT possess a higher $(M-1)_{crit}$ across bias and, despite higher collector doping and avalanche multiplication, improved $V_{CB-crit}$ compared to the second-generation. This trend is good news for common-base safe-operating area in SiGe HBTs with technology scaling. In advanced technology nodes, high Ge concentration and carbon doping

Table 5: Important *ac*, *dc*, and breakdown figures-of-merit for standard-breakdown (HS) devices in second-, third-, and fourth-generation SiGe BiCMOS technologies at 300K.

SiGe BiCMOS Technology	2nd Gen	3rd Gen	4th Gen
peak f_T (GHz)	120	200	300
J_{Kirk} (mA/μm^2)	5.0	12.0	18.0
BV_{CEO} (V)	2.0	1.8	1.7
BV_{CBO} (V)	6.4	5.9	5.6
v_o/r'_b (μA)	15.0	6.9	58.4
r'_e/r'_b nominal	0.20	1.1	0.65
r'_e/r'_b minimum	0.11	0.50	0.33
J_C at min. r'_e/r'_b (mA/μm^2)	0.6	1.5	1.7
min. $V_{CB-crit}$ (V)	2.6	3.1	2.8

prevent boron out-diffusion to obtain a thinner base region for reduced base transit time and improved high-frequency performance. This vertical scaling will result in an increase in the intrinsic base resistance and lower pinched resistance ratio, as is observed in the fourth-generation results compared to third-generation results. It is worth noting that the fourth-generation SiGe HBTs still maintain higher $V_{CB-crit}$ compared to second-generation technology. This suggests that a careful balance between vertical scaling and lateral scaling is required to maintain adequate CB SOA in future SiGe HBT technology generations.

The CB-stability parameters introduced in this research - v_o/r'_b and r'_e/r'_b - describe the bias dependence of $V_{CB-crit}$ and provide physical insight into these often complex breakdown characteristics of advanced SiGe HBTs. For instance, if the intrinsic trigger potential v_o is increased, $V_{CB-crit}$ will more rapidly approach BV_{CBO} as I_E is reduced. If the pinched-resistance ratio r'_e/r'_b is increased, then the value of $V_{CB-crit}$ at high current will be larger. Distinct CB instability regions were identified that display different pinch-in behavior across bias. These regions have an important influence on the bias dependence of the pinched-resistance ratio, the statistical variability of pinch-in, and ultimately on $V_{CB-crit}$ across bias.

Experimental comparisons across different device geometries show that the CB stability parameters do not scale directly with emitter area, so for a fixed current density, larger devices will tend to have a lower $V_{CB-crit}$. This may be an important reliability consideration and potential opportunity for improvement in high-power circuit design. It is also shown that standard variations to transistor layout do not significantly alter the CB-stability characteristics, although layouts with high

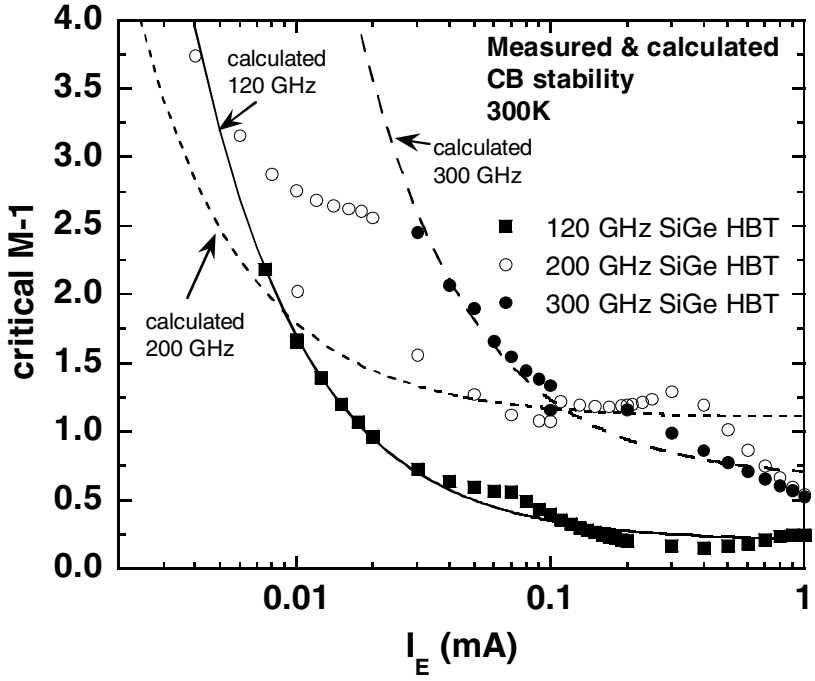

Figure 44: Measured (symbols) and calculated (lines) CB stability thresholds for three generations of SiGe HBT technology.

perimeter-to-area ratio, such as emitter-ring tetrode structures, demonstrate significant improvement in CB stability.

3.4 Operating Voltage Constraints of SiGe HBTs in Extreme Environments

3.4.1 Motivation

The area of "extreme environments," including cryogenic and radiation effects, represents an important niche market for electronics, and SiGe HBT technology shows great promise in terms of reliability and performance outside the domain of conventional operating conditions [44]. However, the role that extreme environments play in breakdown and operating voltage constraints has not been sufficiently investigated. This research focuses on the effects of radiation and cryogenic operation on operational bias and safe-operating area in SiGe HBTs, applying the CB stability analysis methodology introduced in Section 3.3 to experimental data taken for devices operating in extreme environments.

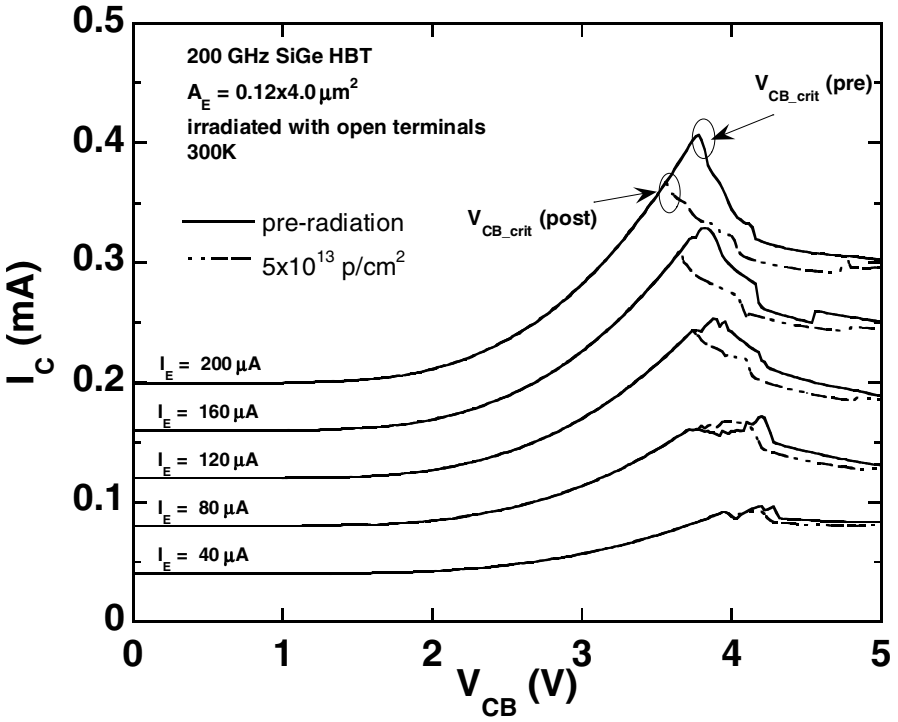

Figure 45: CB-I_E characteristic (I_C) for a device irradiated under floating terminal conditions.

3.4.2 Proton Effects on Operating Voltage Constraints

For space-borne applications, the susceptibility of the electronics to radiation effects is an important concern. An IC technology that in and of itself exhibits "radiation hardness" would possess a clear advantage in this domain [44]. SiGe HBT devices and circuits have been consistently shown to be quite tolerant to total-dose effects from proton, neutron, and gamma irradiation [45]-[48]. An increase in base current is commonly observed for irradiated SiGe HBTs, and is attributed to the creation of G/R trap centers at the E-B spacer Si-SiO_2 interface during radiation exposure [47].

For complete understanding of device and circuit reliability in radiation environments, the role of radiation on transistor operating voltage constraints and breakdown effects should be understood [22]. This section focuses on total dose radiation effects in the context of operational bias and safe-operating area in SiGe HBTs.

For this experiment, the breakdown characteristics during CB-I_E operation were examined on second- and third-generation SiGe HBTs. The *dc* measurements were performed at room temperature using an Agilent 4155 Semiconductor Parameter Analyzer. The samples were passively

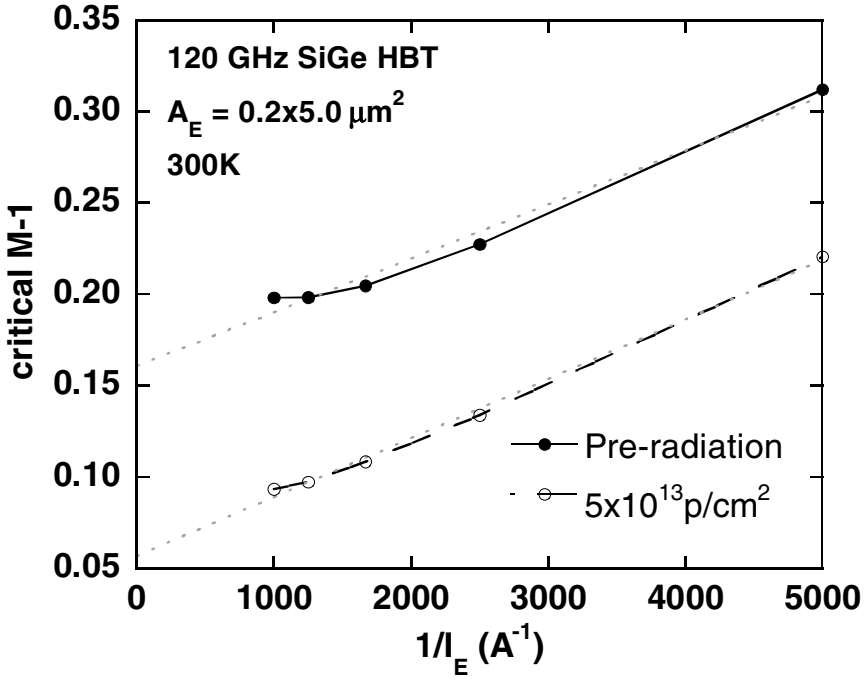

Figure 46: Critical avalanche multiplication factor versus reciprocal emitter current prior to and following proton irradiation at $5 \times 10^{13} p/cm^2$ fluence for a 120 GHz SiGe HBT.

exposed to 63.3 MeV protons in an experiment performed at the Crocker Nuclear Laboratory at the University of California at Davis.

Figure 45 shows a typical CB-I_E characteristic before and after proton exposure. For low voltage conditions (e.g. $V_{CB} < 3.5$ V) no effects are evident. However, at higher V_{CB} a shift in the CB stability threshold ($V_{CB-crit}$) is evident following irradiation. These results are typical for both second- and third-generation SiGe HBTs, and represents a potential reliability concern as the stable operating limits for the device are reduced.

The CB stability analysis technique introduced in Section 3.3 was applied in order to determine the role of radiation on the CB stability parameters r'_e/r'_b and v_o/r'_b. Figure 46 shows the $(M-1)_{crit}$ for a pre- and post-radiated 120 GHz SiGe HBT plotted versus reciprocal I_E, taking the form of Equation 37. With proton exposure, a clear reduction in $(M-1)_{crit}$ occurs across bias. The slope term (v_o/r'_b), which strongly affects CB stability at low currents, appears relatively unchanged following irradiation. However, the y-intercept term (r'_e/r'_b), which influences CB stability at high currents, is significantly reduced.

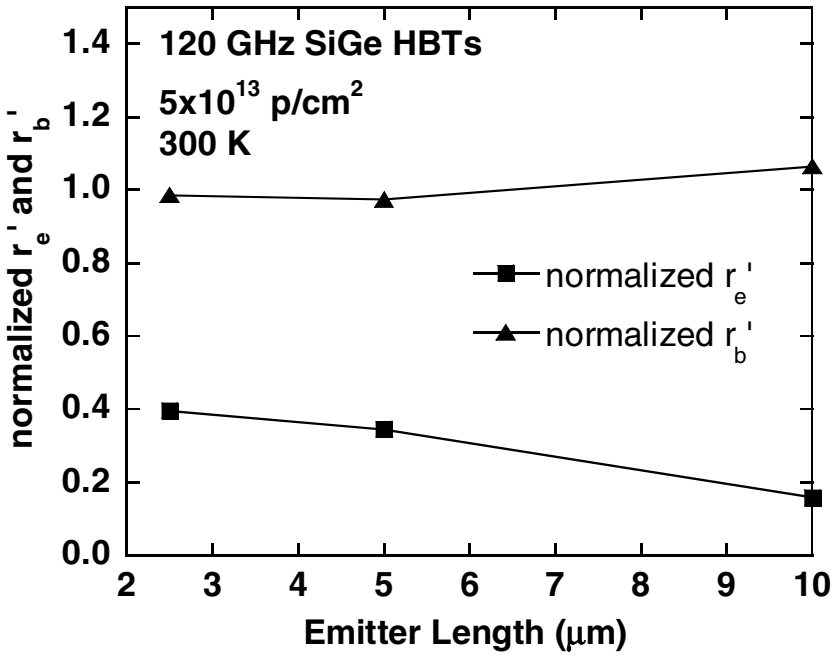

Figure 47: Effective pinched-emitter and base resistances after proton irradiation for 120 GHz SiGe HBTs with different L_E. The plotted values are normalized using the pre-radiation values.

Closer inspection of r'_e and r'_b reveals that r'_b is relatively unchanged during proton exposure, while r'_e is significantly reduced. This is reflected in Figure 47, which shows the post-radiation r'_e and r'_b, normalized by their respective pre-radiation values, for a variety of emitter lengths. This change in r'_e is not believed to be from a substantial change in the actual emitter resistance, but rather a subtle change in the current flow characteristics in the emitter region following irradiation. It is postulated that proton ionization damage at the oxide interface at the emitter-base spacer causes positive charge storage near the emitter periphery [49]. This trapped charge may cause free electrons injected from the emitter to have less tendency to crowd to the center of the emitter, maintaining a lower-resistance state as pinch-in begins to occur in the base.

For all samples examined in both second- and third-generation SiGe HBT technologies, the magnitude of observed degradation to $V_{CB-crit}$ was no more than 0.5 V (approximately 16%) at high current, and negligible at low current. This proves to be a fortunate result for large-signal RF and digital switching circuits, which swing though maximum collector voltage at minimum current. Moreover, because $M - 1$ is not significantly affected by radiation, no degradation to BV_{CEO} or

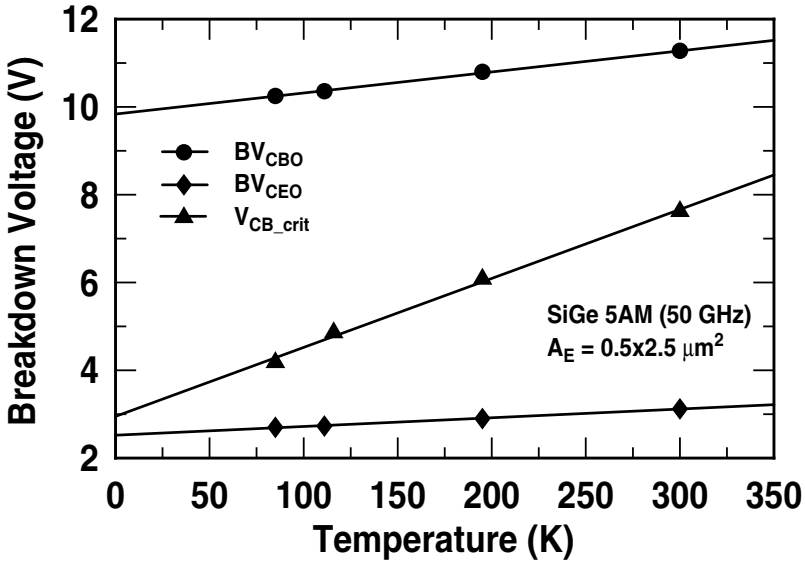

Figure 48: Breakdown voltages across temperature for a first-generation SiGe HBT [23].

BV_{CBO} were observed. These results show that radiation effects pose no devastating consequences to transistor SOA - good news for SiGe HBT device and circuit rad-hard assurance.

3.4.3 Breakdown Effects During Cryogenic Operation

Circuits operating at cryogenic temperatures (e.g. 77 K and below) represent another important area in the broader context of extreme environments. Applications for very low temperature electronics include space-borne systems, high-sensitivity cooled sensors and detectors, and cryogenically cooled computer systems. The performance degradation of Si bipolar homojunction transistors with cooling has been widely reported. However, looking at the position of the thermal energy term (kT) in SiGe HBT device equations, one should expect improvement in a variety of *ac* and *dc* parameters at cryogenic temperatures, including increased current gain (β), Early voltage (V_A), and cutoff frequency (f_T) [44]. This is confirmed in practice, with large improvements in measured performance reported [50].

The role of low-temperature operation of transistor SOA has remained an important question. Figure 48 shows BV trends from 300 K to 85 K for a first-generation (50 GHz) SiGe HBT [23]. The decrease in breakdown voltage with decreasing temperature can be explained by reduced phonon scattering in the Si crystalline lattice. Therefore, the carrier mean free path increases with cooling to

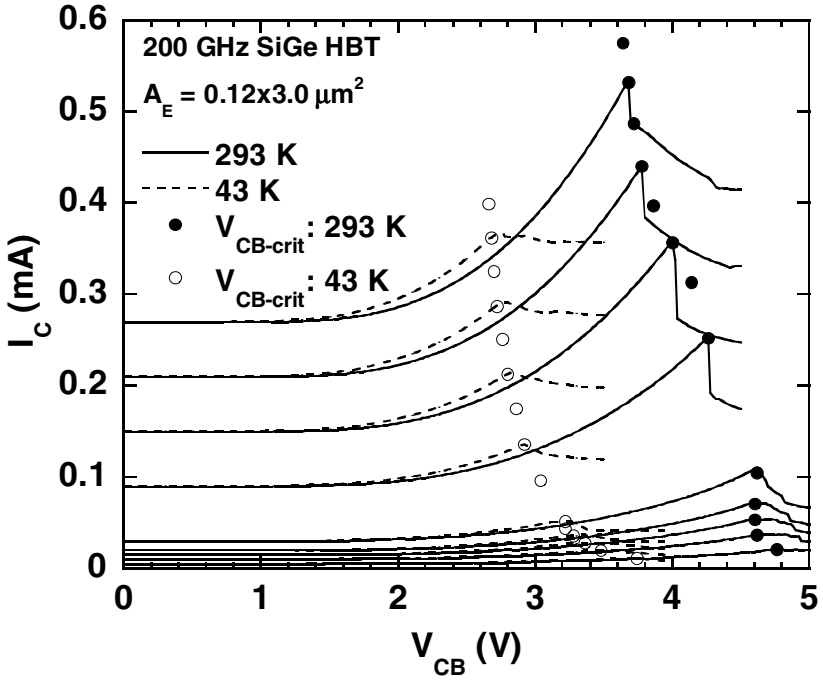

Figure 49: CB-I_E characteristics comparing $V_{CB-crit}$ at room temperature (293 K) and low temperature (43 K) for a third-generation SiGe HBT.

allow electrons to achieve higher kinetic energy prior to lattice collisions, which results in increased impact ionization. However, Figure 48 indicates that the CB pinch-in voltage $V_{CB-crit}$ decreases more rapidly with cooling than either BV_{CEO} or BV_{CBO}. To better understand the role of low temperature on CB stability, the CB-I_E characteristics were measured at temperatures down to 43 K on third-generation SiGe HBTs, and CB stability analysis method introduced in Section 3.3 was applied.

Figure 49 compares the CB-I_E output characteristics for a 200 GHz SiGe HBT at 293 K and 43 K. The pinch-in threshold $V_{CB-crit}$ (circles) shows a substantial decrease across bias at 43 K. Figure 50 shows $(M-1)_{crit}$ as a function of $1/I_E$ at different temperatures. Both the slope and y-intercept of $(M-1)_{crit}$ are observed to steadily decrease as temperature is reduced, indicating that both the pinch-resistance ratio (r'_e/r'_b) and the avalanche trigger (v_o/r'_b) are affected by cooling. This decrease in the avalanche trigger with cooling is attributed to a significant increase in the low-current value of r'_b. As I_E increases the magnitude of r'_b change across temperature is much less dramatic. These results are consistent with the effects of carrier freezeout on base resistance

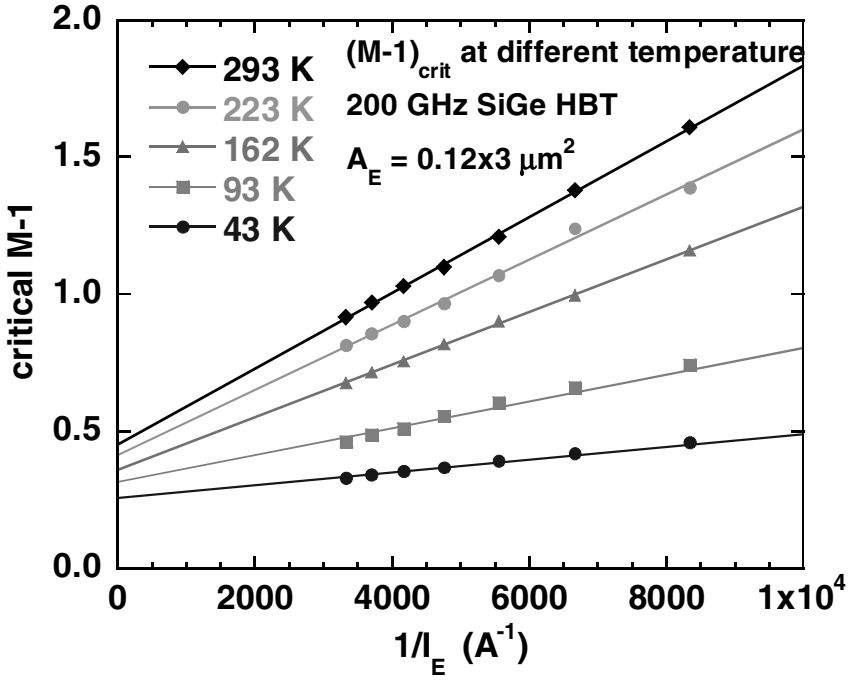

Figure 50: Critical $M-1$ as a function of reciprocal I_E for a third-generation SiGe HBT at different ambient temperatures.

and conductivity modulation, the latter of which has been reported to be more pronounced under cryogenic conditions [51], [52]. In addition, the effective emitter resistance during pinch-in (r'_e) was observed to decrease at low temperature, a change attributed to carrier mobility enhancement in the highly doped emitter. As a result, the negative feedback influence of $r'_e I_E$ to suppress pinch-in is reduced, lowering the pinched-resistance ratio r'_e/r'_b and ultimately lowering $V_{CB-crit}$ across bias.

The CB stability parameters are summarized across temperature in Figure 51, where normalized (at 293 K) values of $V_{CB-crit}$, r'_e/r'_b, $M-1$, r'_b and r'_e are plotted as a function of temperature for $I_E = 0.3$ mA. The 30% increase in $M-1$ with lower temperature contributes to the decrease in $V_{CB-crit}$. More importantly, however, are the changes in both r'_e and r'_b, which result in significant degradation of $(M-1)_{crit}$ as T is reduced. As Figure 51 shows, at higher current the 60% decrease in r'_e is the largest contributing factor to the reduction of $(M-1)_{crit}$ at low T, and thus is the primary source of $V_{CB-crit}$ degradation.

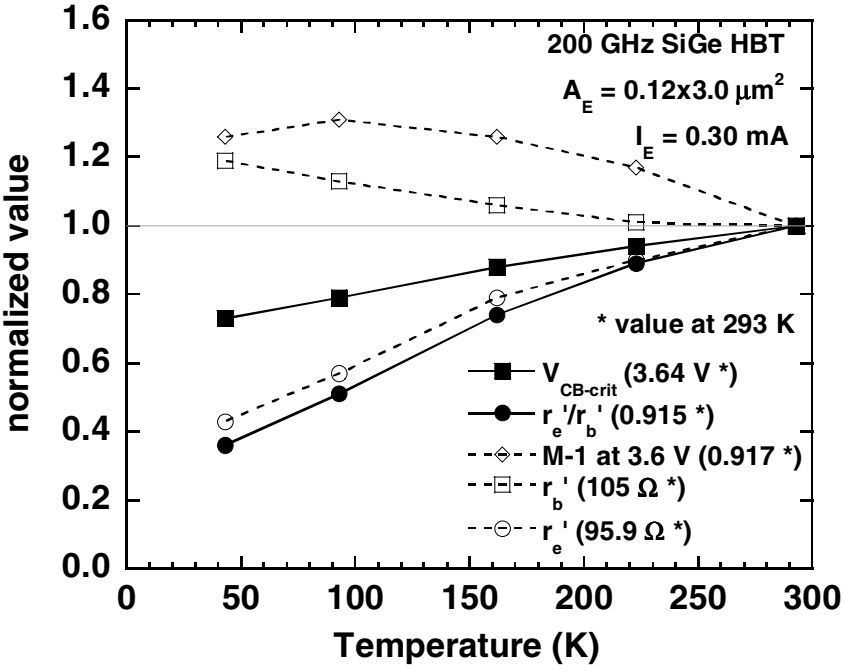

Figure 51: Important CB-stability parameters (normalized at 293 K) across temperature: $V_{CB-crit}$, r'_e/r'_b, $M-1$ for fixed V_{CB}, r'_b, and r'_e.

3.4.4 Summary

For the first time, the effects of high-energy protons and cryogenic operation on CB avalanche effects in SiGe HBTs were studied to evaluate CB safe-operating area in extreme environments. It was shown that in both cases the pinch-in voltage $V_{CB-crit}$ degrades, introducing potential reliability concerns for circuits operating in the these environments. For irradiated SiGe HBTs, the modest degradation observed was attributed to a decrease in the ballasting r'_e following irradiation. For cryogenic operation, the degradation is more pronounced because a combination of factors; lower r'_e, higher r'_b, and higher $M-1$ all contribute to decreasing $V_{CB-crit}$.

CHAPTER IV

RF OPERATING LIMITS IN SIGE HBTS

4.1 Introduction

The power amplifier (PA) represents a key building block in RF front-end modules. Despite the attractive thermal and reliability properties SiGe HBTs possess compared to GaAs HBTs, SiGe technology faces fundamental challenges in the area of PA development [53]-[55], particularly as transistor performance is pushed upwards in frequency. Therefore, a key challenge in SiGe HBT PA design is obtaining high output power density because of the smaller bandgap and lower breakdown voltage of SiGe HBTs compared to many III-V HBTs, which limits the maximum collector voltage bias and output dynamic voltage swing. To maintain adequate output power at high frequencies several strategies are possible.

1) Use a higher breakdown device, with the penalty of lower gain and lower efficiency for applications at higher frequencies.

2) Increase the maximum current swing by using larger transistor area or more transistors in parallel that require power-combining. This comes at the expense of lower input and output impedances, which can prove difficult to match while maintaining adequate frequency bandwidth [56]. In addition, increasing the complexity of the on-chip matching and power-combining networks generally translates to larger die area and higher losses in the integrated lines and passives due to the lossy nature of the silicon substrate.

3) Operate at higher collector voltage to increase the maximum voltage swing. This approach comes cost of potentially decreased reliability.

A cascode PA topology can serve as a viable strategy to simultaneously increase RF gain and maximum collector voltage for higher output power [6]. A clear understanding of the voltage operating limits and associated implications to large signal performance and reliability is necessary to achieve the desired power performance for robust high-frequency operation.

After examining the *dc* operating limits in Section 4.2 for the particular cascode SiGe HBT under study, this chapter will focus on three different reliability and performance aspects of aggressive collector voltage bias on cascode SiGe HBT PA core operation. Section 4.3 examines the transistor RF performance in the region of base current reversal. Section 4.4 investigates the effects of RF stress under these aggressive bias conditions. Section 4.5 examines transistor failure limits under high bias voltage and large-signal RF conditions to determine the RF safe-operating area (SOA) for cascode SiGe HBT PA cores.

4.2 Voltage Constraints During Cascode Operation

The *ac* cascode structures examined for this study use high-performance (HS) 200 GHz SiGe HBTs fabricated in a third-generation SiGe BiCMOS process [57]. The *dc* characteristics and schematic of the cascode SiGe HBT power amplifier core used in this study are shown in Figure 52. In this cascode configuration the RF input is applied to the base terminal of Q1 while the collector terminal of Q2 serves as the RF output. Both SiGe HBTs are sized at 0.12x18 μm^2 and have an open-base breakdown voltage (BV_{CEO}) of 1.8 V and collector-base junction breakdown voltage (BV_{CBO}) of 5.9 V. The base voltage for Q2 is set at 1.8 V to maintain forward-active operation of Q1 while minimizing the knee-voltage (V_{Knee}) of the cascode pair. In this scenario, the voltage across the collector-base junction of Q1 remains low (0.2 V or less). However, the voltage limits of Q2 are an important concern, and this transistor will undergo collector-base junction breakdown for V_C exceeding 7.7 V.

The *dc* operation of the cascode pair is in many ways similar to CB-I_E operation discussed in Chapter 3, since the lower device Q1 provides a near constant emitter current drive to the upper device Q2. As V_C increases, avalanche multiplication in the collector-base space-charge region (CB-SCR) of Q2 increases the collector current and reduces its base current, and when V_{CE} for Q2 exceeds BV_{CEO} the sign of I_{B-Q2} reverses as avalanche holes exit the upper-base terminal [32], [35]. The dashed line in Figure 52 (near $V_C = 3$ V) indicates the position where base current reversal (BCR) occurs for the top device.

As the magnitude of reverse base current increases with V_C, the voltage drop across the distributed base resistance can lead to current crowding at the center of the transistor. This mechanism

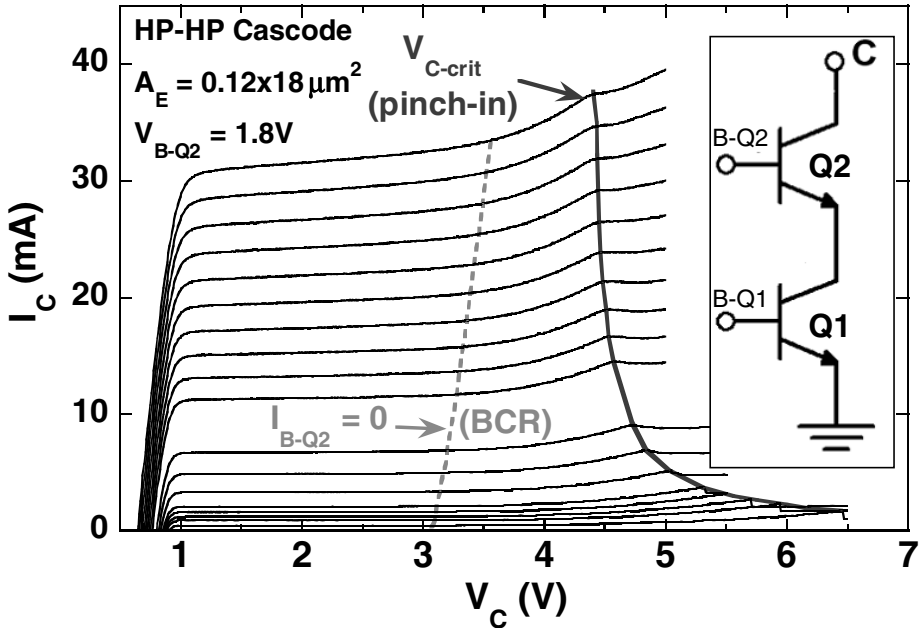

Figure 52: The *dc* output characteristics for the cascode power core as V_{B-Q1} is increased from 0.8 to 1.02 V with V_{B-Q2} fixed at 1.8 V. The collector voltage thresholds for base-current reversal (BCR) (for Q2) and pinch-in are indicated.

can result in instabilities in the *dc* characteristics, which are often referred to as pinch-in effects, when V_C exceeds the critical value V_{C-crit} [34]. Due to the avalanche-induced instabilities associated with pinch-in, V_{C-crit} is considered to be the upper limit for stable device biasing during common-base and cascode operation [20].

4.3 RF Performance of Aggressively Biased Cascode SiGe HBTs

4.3.1 Experimental Setup

The effects of aggressive collector voltage bias on the RF power and linearity performance of cascode SiGe HBTs was examined using single- and two-tone measurements at various collector voltages. Using a Maury load pull system with automatic source and load impedance tuners, stepped power measurements were performed at 10.5 GHz on the cascode power cell as V_C was varied from 3 V to 4.8 V to determine the effects of strong base current reversal and pinch-in ($V_C > V_{C-crit}$) on power performance. The source and load impedances were tuned to obtain maximum P1dB at $V_{B-Q1} = 0.89$ V and $V_C = 4$ V. Measurements were taken for both Class A ($V_{B-Q1} = 0.89$ V) and Class AB ($V_{B-Q1} = 0.8$ V) operation. The two-tone measurements used a 1 MHz tone spacing.

4.3.2 Results and Discussion

Figure 53 shows Class A gain as a function of collector voltage as RF input power is varied. During these measurements the collector current was observed to increase from approximately 8 mA to 22 mA as input power was increased from -24 dBm to -8 dBm as the device self-biases with increased RF power. Under these bias conditions the impedance-matched cascode power core demonstrates a gain slightly greater than 25 dB at 10.5 GHz. At higher input power the effects of gain compression are clearly shown, particularly for lower voltage operation since the dynamic voltage swing becomes distorted as its lower limit clips at the knee voltage. Operating at higher V_C in the region of significant BCR shows no observable effect on gain performance until the device bias approaches V_{C-crit} where a moderate fluctuation in gain is observed as the operating point begins to cross into the region of pinch-in instabilities.

Figure 54 shows the output-referred 1-dB compression point (OP1dB), the power added efficiency (PAE), and the output-referred third-order intercept point (OIP3) as a function of collector voltage bias. Raising V_C from 3 V to 4 V provides considerably more output power, with P1dB increasing by 4.5 dB, despite operating in the region where avalanche effects and BCR are significant. Likewise, an increase in the peak PAE from 26% to 32% is observed as V_C is increased. Intermodulation distortion was evaluated by a two-tone measurement at P_{in} = -20 dBm, which is considerably backed off from P1dB. The device shows a substantial variation in linearity across V_C as indicated in Figure 54 by the OIP3 result, which peaks around 21.3 dBm and drops as low as 16.9 dBm at high V_C because of avalanche nonlinearities. Despite this degradation, this result shows that peak linearity performance is obtained under conditions of significant base current reversal, and that biasing near to or even beyond the pinch-in stability threshold shows no devastating impact to linearity performance.

The enhancement to output power and PAE resulting from aggressive collector voltage bias demonstrate the RF performance benefits of operating the cascode power core into the region of strong avalanche effects. However, the effects of cumulative stress degradation and catastrophic device failures for large-signal RF operation at high V_C pose important reliability concerns and will be addressed in the following sections.

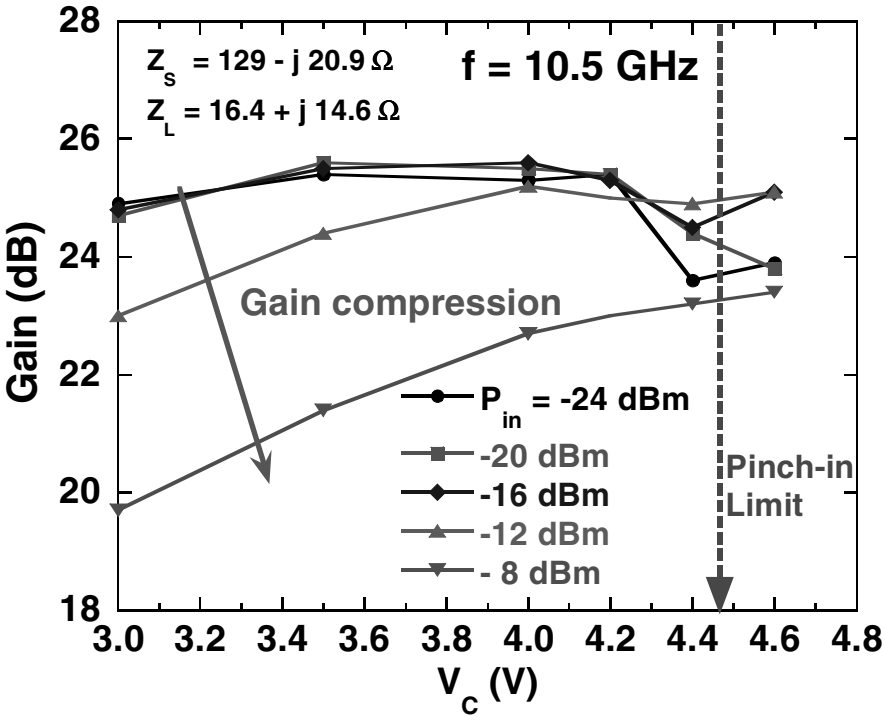

Figure 53: Gain as a function of V_C at different RF input power for the power-matched cascode power core at 10.5 GHz.

4.4 Reliability of Aggressively Biased Cascode SiGe HBTs

4.4.1 Experimental Setup

Several measurements were performed to examine the effects of dynamic stressing on the *dc*, power, and linearity characteristics for the cascode power cores. Using the source and load impedance tuners on the Maury load pull system, the source and load impedances were tuned at 9.5 GHz for maximum output power, and a fresh device was measured to determine the RF and *dc* characteristics prior to stressing. Next, a CW signal at 9.5 GHz was applied to the input of the matched PA core for time intervals up to 39,600 seconds (11 hours). A variety of stress conditions were examined, including bias at different V_C up to the V_{C-crit} limit around 5 V and RF input power of -10 dBm (near the 1-dB compression point) and 0 dBm (overdrive past P1dB). Stressing was periodically interrupted to characterize the devices. A *dc* measurement, similar to a Gummel characteristic but performed on the cascode pair, was used to measure the excess base current degradation resulting

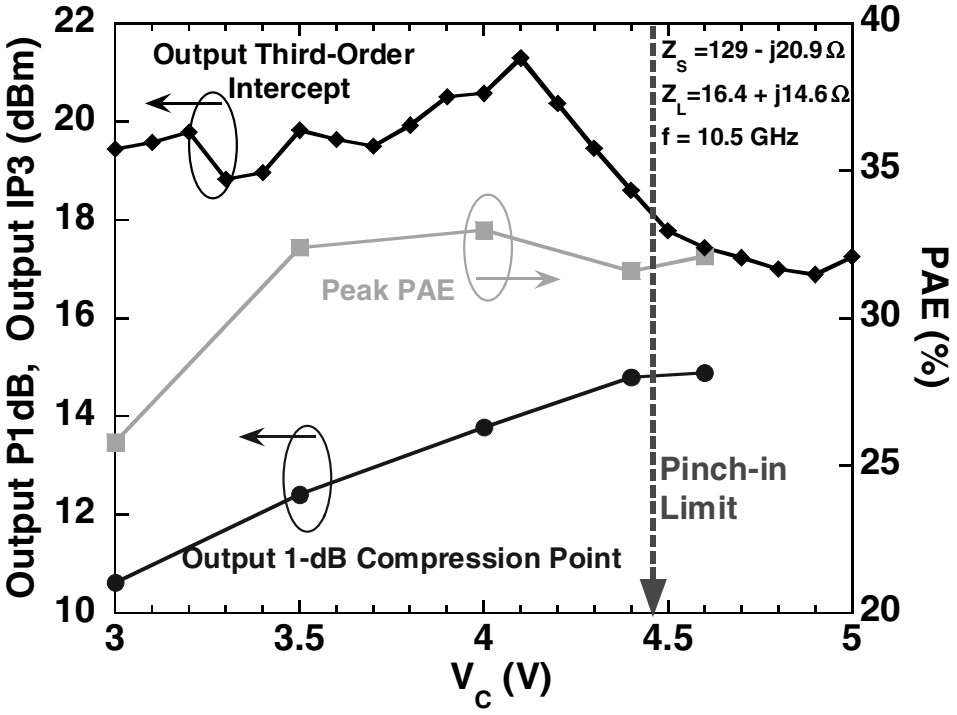

Figure 54: Comparison of output 1-dB compression point, output third order intercept point, and peak PAE across collector voltage for the cascode power core at 10.5 GHz.

from RF stressing. V_{B-Q1} and V_{B-Q2} were swept together such that (assuming negligible device-to-device mismatch) V_{BE} for each remains approximately equal (e.g. $V_{B-Q2} = 2\text{x}V_{B-Q1}$). Due to *dc* SMU limitations, V_C could not be simultaneously swept to maintain constant V_{CB}, so V_C was fixed at 2 V. This V_C condition was determined to have no impact on the extraction on excess base current.

4.4.2 Results and Discussion

Figure 55 shows the cascode "Gummel" characteristics prior to and following 36,000 seconds (10 hours) of RF stress (9.5 GHz) at P_{in} = -10 dBm (approximately P1dB for the matched power core). During stress the collector was biased at 4 V and the collector current was 16.6 mA. The RF stress resulted in a considerable increase of the base current of the top transistor (Q2) while no significant change was observed for I_{B-Q1} [24]. This behavior appears consistent with the mix-mode reliability damage mechanism, where hot avalanche carriers generated in the collector-base space charge region create interface traps at the E-B spacer and shallow trench edge under *dc* conditions

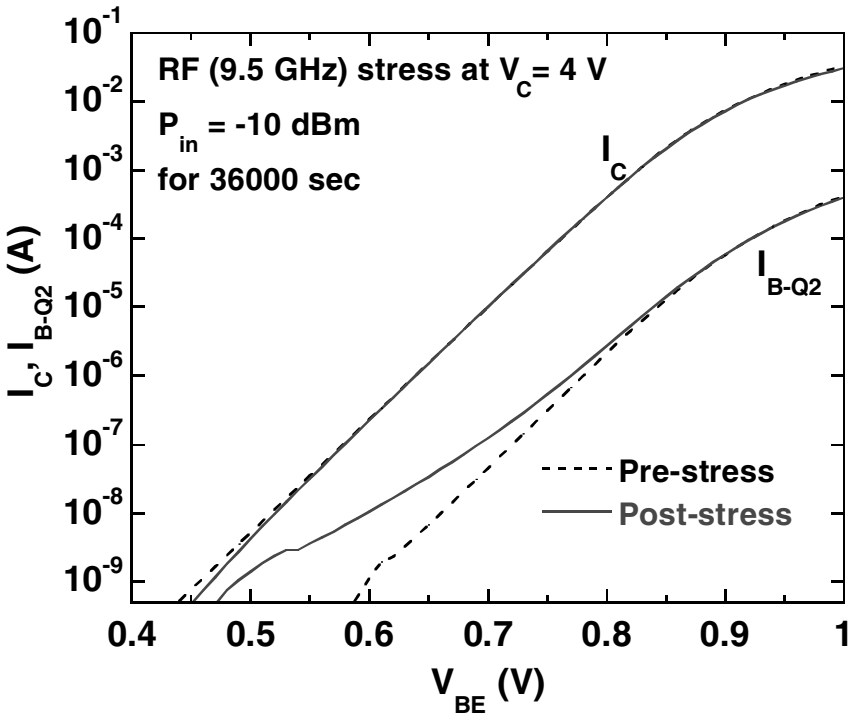

Figure 55: Gummel characteristics (I_C and I_{B-Q2}) on cascode power core before (dashed line) and after (solid line) 36,000 seconds RF stressing at 9.5 GHz with Pin = -10 dBm and V_C = 4 V.

of simultaneous high J_C and high V_{CB} operation [58]. These trap states result in an increase in the base current recombination rate and thus higher non-ideal base current. Although both HBTs in the cascode pair are subject to the same J_C, the top transistor Q2 can be expected to undergo significantly more hot-carrier damage compared to Q1 because the V_{CB} of Q2 is 2.2 V and it undergoes a wide output dynamic voltage swing [59].

The excess base current following stress ($[I_{B-post-stress} - I_{B-pre-stress}]/I_{B-pre-stress}$) was extracted from the Gummel at V_{BE} = 0.65 V, normalized to the pre-stress value, and plotted as a function of accumulated stress time for a variety of stress conditions in Figures 56 and 57. Figure 56 shows the measured I_B degradation following RF stress at 0 dBm for the collector voltages ranging from 1.8 V (V_{CB-Q2} = 0 V) to 5 V (V_{CB-Q2} = 3.2 V). At V_C of 4 V and 5 V, RF stressing at -10 dBm is also shown for comparison. In all cases, the magnitude of damage tends to increase for longer stress time, although a decrease in the damage rate is observed after the first 10 seconds of stress. This is attributed to a trap-annealing mechanism caused by self-heating in the device that removes a portion of the damage as it is being generated [60].

Interestingly, Figure 56 shows that for RF stress at V_{CB-Q2} = 0 V (V_C = 1.8 V) damage eventually becomes apparent over long enough stress time (past 100 s), while *dc*-only mix-mode stressing exhibits virtually no increase in non-ideal base current for V_{CB} = 0 V [58]. This difference explicitly highlights the contribution of the dynamic voltage swing to the overall stress damage [59]. Overall, the experimental results shown in Figure 56 show that operating at higher V_C tends to result in higher levels of damage as indicated by the increase in excess base current. However, a strong increase in damage is not observed by increasing V_C from 4 V to 5 V. In addition to higher junction temperature for V_C = 5 V, transistor Q2 is operating in the pinch-in region, and central current crowding can result in lower damage by decreasing the avalanche multiplication rate and increasing the distance between the avalanche generation and the E-B spacer and trench oxide [59], [61]. Furthermore, comparing the results in Figure 56 for stress at P_{in} = -10 dBm and 0 dBm shows that higher input power drive will result in higher levels of damage due to the increased dynamic voltage and current swings.

For additional insight into the role of *ac* versus *dc* stress on these cascode SiGe HBTs, Figure 57 compares the excess base current for RF stress (at 0 dBm) with *dc*-only stress for V_C = 5 V. In addition to the standard stress case "P_{in} = 0 dBm, I_C = 28 mA", the low-current "No RF, I_C = 8 mA" case uses the standard bias condition of V_{BE} = 0.89 V. The high-current "No RF, I_C = 28 mA" case uses higher V_{BE} in order to match the I_C observed in the standard case when the cascode is driven by P_{in} = 0 dBm. An additional low-current case ("0 dBm, I_C = 8 mA") applies RF stress in the same manner except the bottom transistor is driven with a constant base current rather than constant V_{BE} so that I_C is fixed at 8 mA and will not increase due to the RF input power. The damage during RF stress is at least two times greater than damage for *dc*-only stress for both low- and high- current cases. The rate of damage with time is steady for both cases of low-current stress, but tends to decrease after 10 seconds during both cases of high-current stress because of thermal-induced trap annealing.

Since the load impedance (Z_L) presented to the cascode core will directly influence its dynamic output swing, one should expect that the device degradation observed during large-signal RF operation to be directly affected by Z_L. This is clearly the case, as indicated in Figure 58, which shows the *dc* degradation due to RF stress at 9.5 GHz for three different load impedance match conditions.

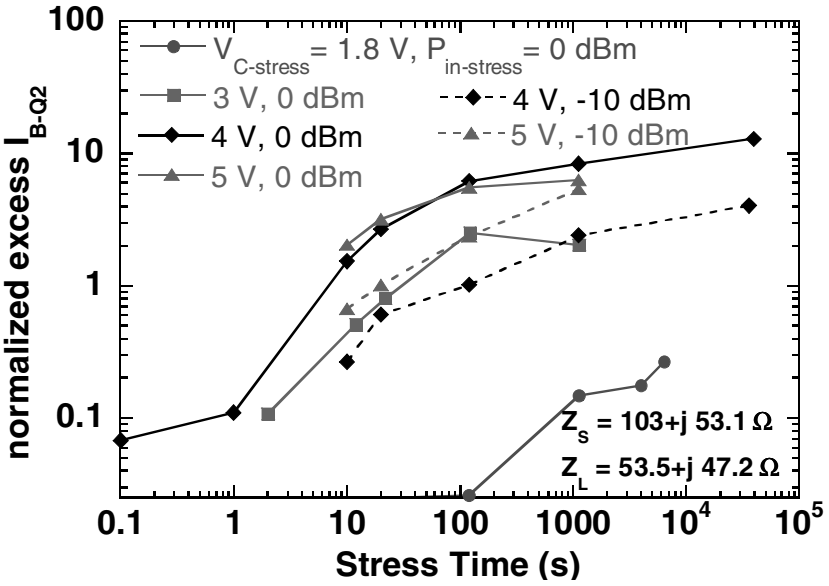

Figure 56: Normalized Q2 excess base current (extracted at V_{BE} = 0.65 V) as a function of RF stress time (CW at 9.5 GHz) for a variety of stress conditions. Source and load impedances were matched for optimal power.

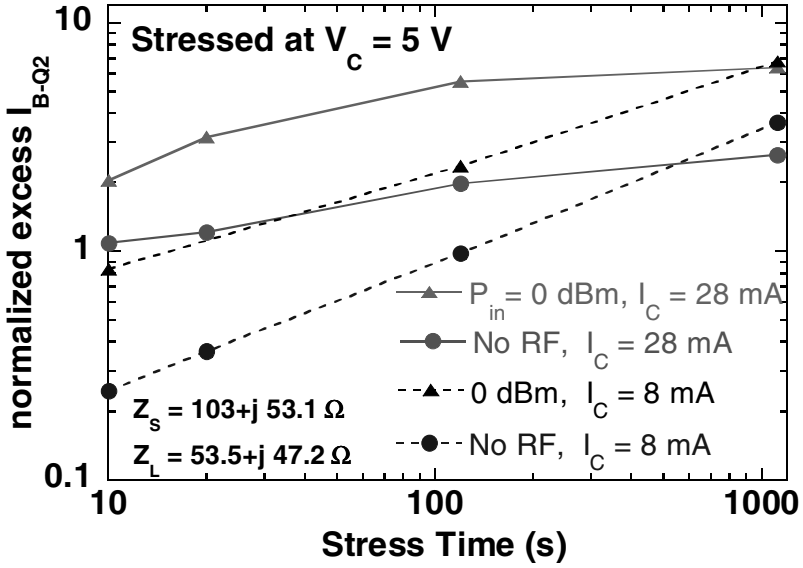

Figure 57: Normalized Q2 excess base current (extracted at V_{BE} = 0.65 V) as a function of RF stress time (CW at 9.5 GHz) for RF (0 dBm) and *dc*-only stress at low- and high-current conditions. The collector voltage is 5 V during stress and source and load impedances were matched for optimal power.

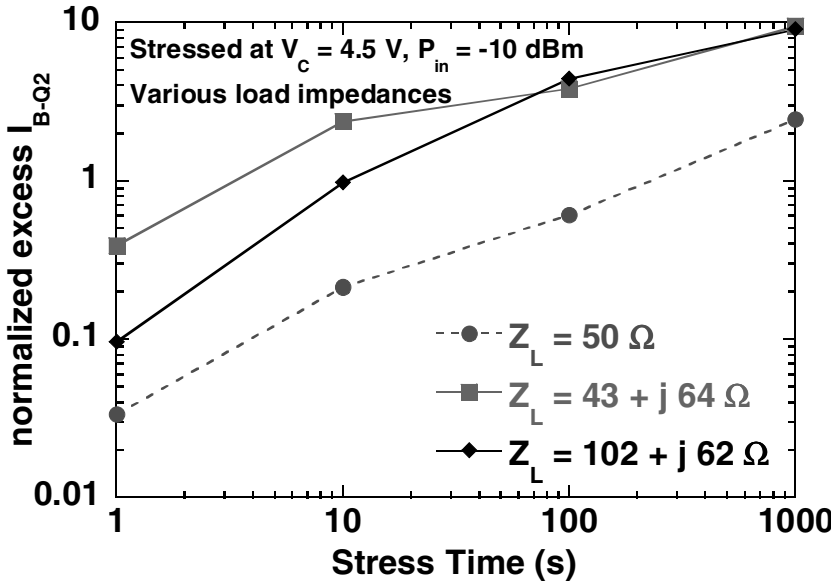

Figure 58: Normalized Q2 excess base current (extracted at V_{BE} = 0.65 V) as a function of RF stress time (CW at 9.5 GHz) for RF input power of -10 dBm at various load impedance conditions. The collector voltage is 4.5 V during stress.

For $Z_L = 43 + j64\ \Omega$, the gain is highest (24.5 dB), resulting in a higher output voltage swing and a higher degree of damage. For $Z_L = 50\ \Omega$, the gain (and P_{out} for fixed P_{in} = -10 dBm) is about 4 dB lower, and the subsequent damage is observed to be considerably lower. Physical modeling of this RF damage mechanism, which accounts for load impedance while predicting trap generation within the device, is discussed in [59].

Given the *dc* degradation observed during RF stress, the subsequent effects on the power and linearity characteristics of SiGe HBT cascode stages are of interest. Previous studies have reported on the effects of hot-carrier (HC) stress on *ac* and power performance in SiGe HBTs, and demonstrate that changes to RF characteristics are observed primarily during measurements at fixed I_B (bias point changes with I_B degradation), while pre- and post-stress comparisons at fixed I_C show only small changes in performance [62], [63]. The case can be made that the cascode topology using aggressive V_C bias is largely immune to the effects related to I_B degradation since β for the top transistor is not a critical parameter for the circuit (and the top transistor is biased in BCR). Also, degradations to linearity and PAE resulting from dynamic stress have been reported for CMOS devices because of degradation in transconductance, overlap capacitances, and gate resistance [64]. Clearly,

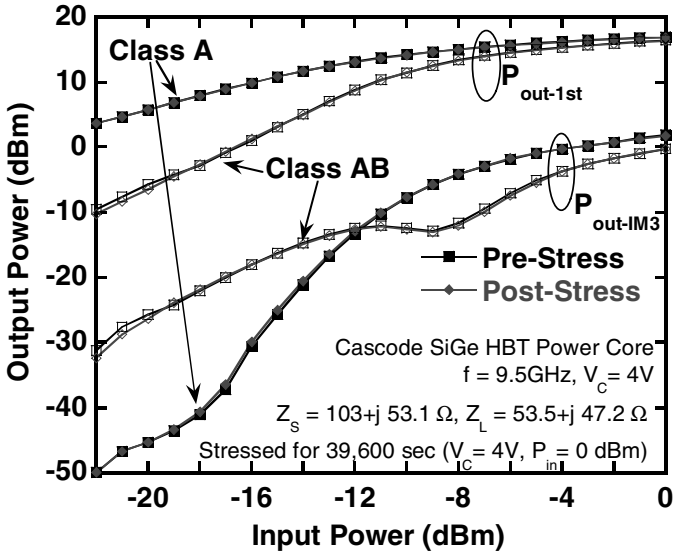

Figure 59: Class A and Class AB fundamental output power ($P_{out-1st}$) and third-order intermodulation distortion ($P_{out-IM3}$) before and after 39,600 seconds RF stress (CW at 9.5 GHz) with P_{in}=0 dBm and V_C=4 V. Z_S and Z_L were tuned for optimal power during both stressing and characterization.

the damage mechanism and performance implications will differ significantly between CMOS and SiGe HBT devices, but the impact of stress on RF performance for SiGe HBTs should be investigated.

Figure 59 shows the output power ($P_{out-1st}$) and third-order intermodulation ($P_{out-IM3}$) characteristics for the matched cascode stage at 9.5 GHz before and after 39,600 seconds of RF stress (V_C = 4 V, P_{in} = 0 dBm). These results show virtually no change to to fundamental or third-order intermodulation output powers, indicating that gain and linearity do not degrade for either Class A or Class AB operation. Past P1dB, output power is slightly lower after stress (by approximately 0.1 dB), causing peak PAE to drop by about 1.2% for both Class A and Class AB operation, as shown in Figure 60. This decrease may be from a slight offset of the optimal match condition caused by stress, although limitations of measurement accuracy and probe contact cannot be ruled out for this slight variation. Overall, prolonged RF stress in regions of strong BCR shows very little impact on the power and linearity performance of cascode SiGe HBT power cells, despite *dc* degradation to base current for the top transistor. A model and methodology for extracting power core operating lifetime based on this RF damage mechanism and design-specific criteria is discussed in [65].

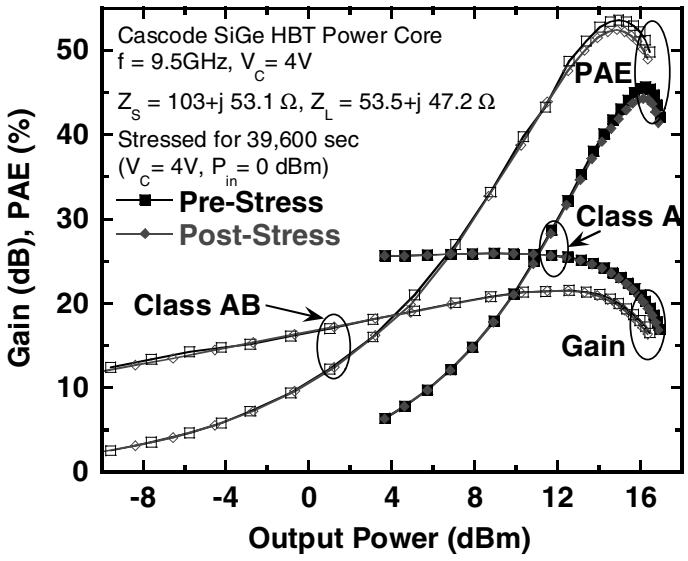

Figure 60: Class A and Class AB gain and PAE before and after 39,600 seconds RF stress (CW at 9.5 GHz) with P_{in}=0 dBm and V_C=4 V. Z_S and Z_L were tuned for optimal power during both stressing and characterization.

4.5 Large-Signal RF Safe-Operating Area of Cascode SiGe HBTs

4.5.1 Experimental Setup

The onset of catastrophic device failure under conditions of high RF power and high collector voltage bias was studied on cascode SiGe HBTs using stepped RF stressing. For a given V_C bias and load impedance, a brief (approximately 1 second) low-power CW signal at 9.5 GHz was applied to the input of the SiGe PA core. An I-V sweep was performed to monitor the *dc* characteristics of the device following the RF stress. RF power was stepped by 1 dB (or smaller) increments and the test repeated until the device showed signs of failure. Using the Maury impedance tuners. this experiment was repeated for a variety of load impedances, and V_C was varied between 4 V and 6 V to examine this failure mechanism in the bias region beyond V_{C-crit}. Timed stress measurements were also performed at constant input power up to 1000 s. In total, over 100 identical power cores were stressed to the point of failure during the course of these experiments. Similar measurements were also performed on larger devices that were each comprised of four of the standard (devices with emitter area of 0.12x18 μm^2) cascode power cores in parallel.

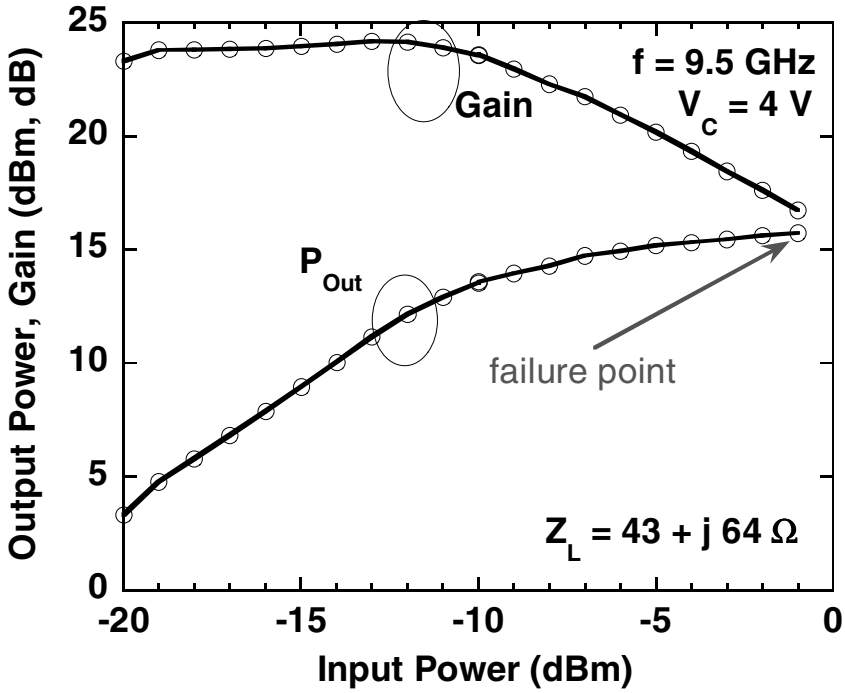

Figure 61: Output power and gain vs. input power for different V_C on the cascode power core. The RF power at which the device undergoes catastrophic failure is indicated for each V_C.

4.5.2 Damage Characteristics During RF Failure

At high collector voltage bias, catastrophic failure of the SiGe HBT can occur when excessive RF power is applied. This failure point ($P_{Out-Fail}$) is indicated in Figure 61 for the SiGe HBT cascode power core biased at V_C = 4 V. The load impedance (Z_L) of 43 + j64 Ω was selected for optimal high-power match based on measured load-pull results at 9.5 GHz.

To examine the onset of this failure mechanism, RF power was carefully stepped in 0.1 dB increments near $P_{Out-Fail}$, and after each stress point the *dc* characteristics were remeasured. During the *dc* measurement the collector voltage is held constant at 2 V while the base voltages for Q1 and Q2 are swept simultaneously. These results are shown in Figure 62 for a cascode SiGe HBT PA core stressed while V_C was held at 5 V. Both the unstressed device and the device stressed at low RF power (-10 dBm) show a normal collector current dependence with V_{BE}. However, as RF power is gradually increased beyond the failure threshold, the collector current indicates the onset of a reverse CB junction leakage current for the output transistor Q2. This leakage becomes more pronounced

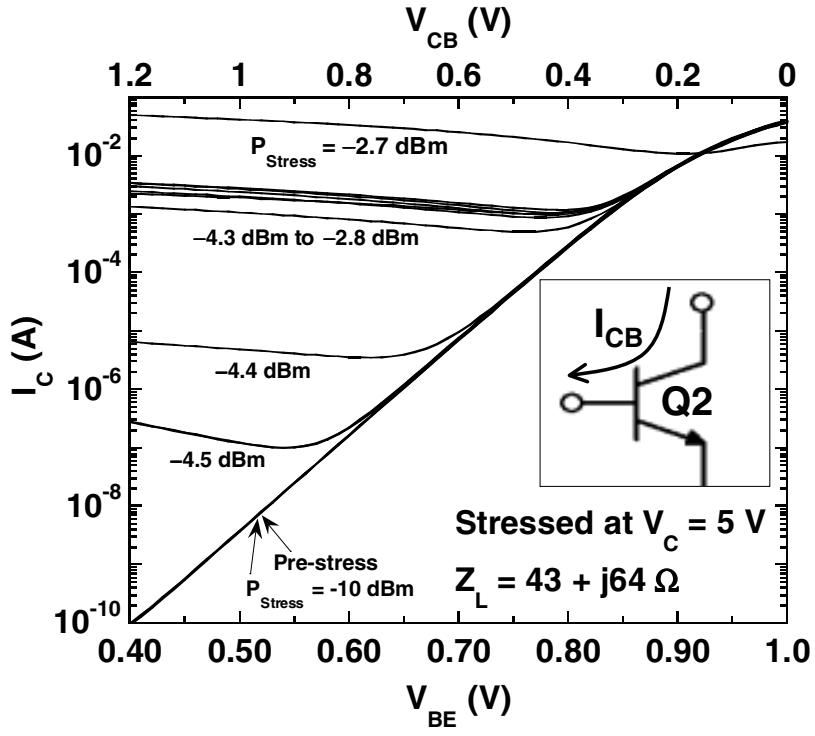

Figure 62: Collector current as a function of V_{BE} and V_{CB} showing CB junction leakage current attributed to damage during RF stress at $V_C = 5$ V for different input power.

as RF power increases until the transistor is nonfunctional. The CB junction leakage current (I_{CB}) is extracted and plotted as a function of RF stress power in Figure 63. At the onset of damage (around 5 dBm in Figure 63) an exponential dependence of I_{CB} across V_{CB} is observed, suggesting a trap-induced tunneling damage mechanism at the CB junction of Q2. As RF power is increased beyond this threshold, I_{CB} becomes linear with respect to V_{CB}, indicating that an accumulation of a large number of traps has effectively shorted the CB junction. When this occurs, the I_C of Q2 is primarily independent of its I_E and the transistor is no longer functional.

Additional measurements were performed following RF stress at various time intervals up to 1000 seconds to determine the role of cumulative stress time on CB junction damage. These results shown in Figure 64 indicate that damage to the CB junction does not accumulate for stress below a certain RF power threshold, regardless of stress time.

The point at which a device will fail under large-signal RF conditions depends on a variety of

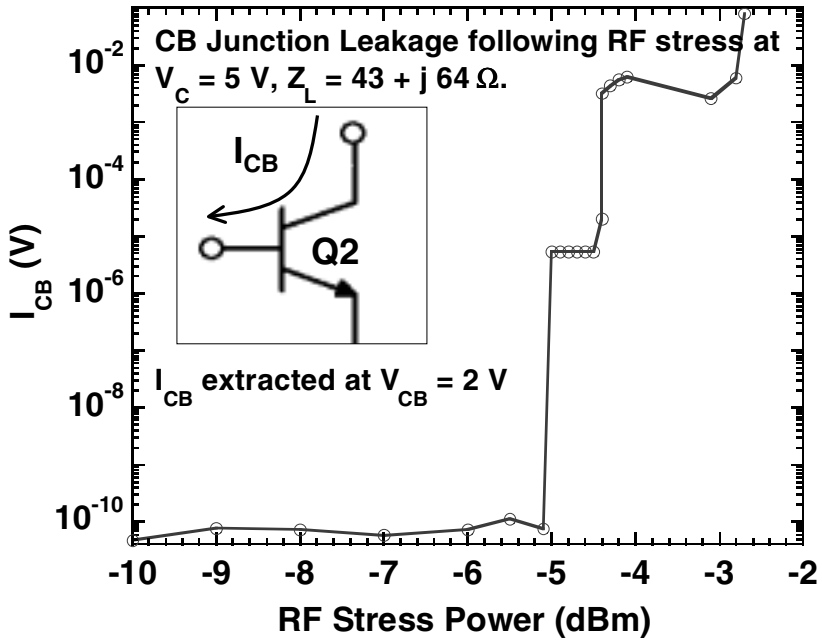

Figure 63: CB junction leakage current extracted at V_{CB} = 2 V for a cascode power core stressed at various RF power.

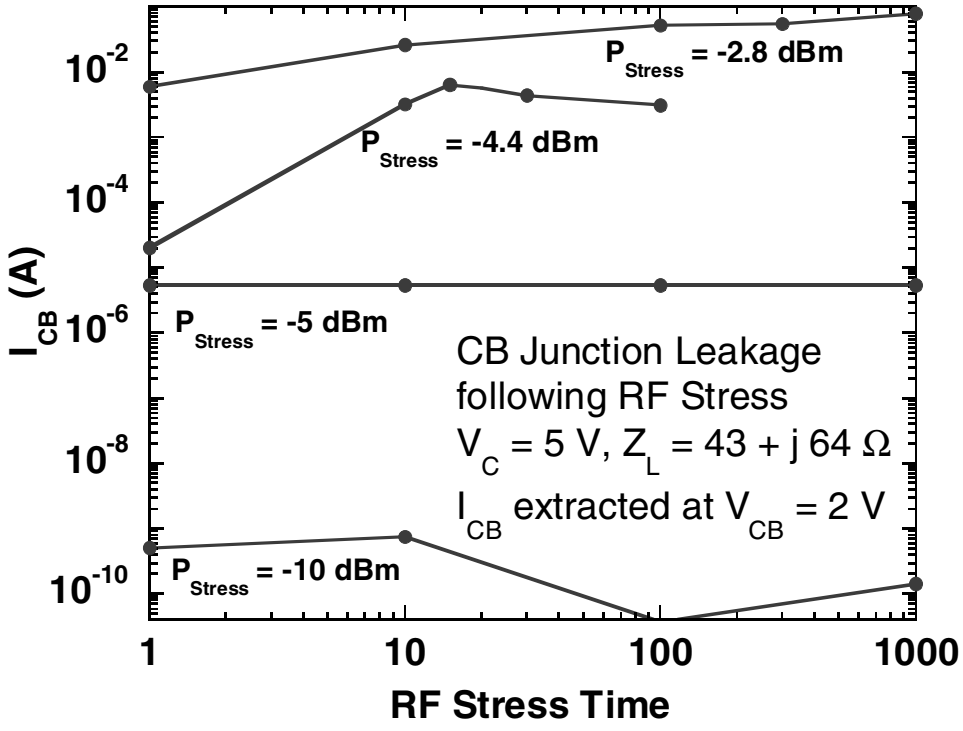

Figure 64: CB junction leakage current extracted at V_{CB} = 2 V as a function of cumulative stress time for a cascode power core stressed at various RF power.

factors, including *dc* collector voltage (V_C), load impedance (Z_L), and the breakdown of the output transistor (Q2). The dynamic SOA limit will be examined in this section for two distinct cases: a) dynamic voltage limits related to CB junction breakdown, and b) dynamic current limits related to excessive operating current densities and pinch-in effects.

4.5.3 Voltage-Limited Dynamic SOA Results

Failure at the CB junction will occur during RF operation when the maximum dynamic output voltage swing exceeds the limit V_{Fail}, which is related to BV_{CBO} of Q2 for the cascode power core: $V_{Fail} \approx (1+\chi)BV_{CBO} + V_{B-Q2}$ for $0 < \chi < 0.1$. This scenario is depicted graphically in Figure 65 for $Z_L = 43 + j64\ \Omega$ (the same load used in Figure 61) at two different V_C bias conditions. The dynamic I-V characteristics were calculated based on experimental $P_{Out-Fail}$ results, and compared with harmonic balance simulation results using the design kit model. The dynamic voltage limits V_{Fail} and V_{Knee} are indicated. Considering the maximum dynamic voltage limit V_{Fail}, a reduction in $P_{Out-Fail}$ is expected as V_C bias increases. For comparison, and different load condition ($Z_L = 395 - j16\ \Omega$) with a larger resistive component and small reactive component is shown in Figure 66. As indicated, a larger load resistance is expected to increase the magnitude of the voltage swing and thus decrease $P_{Out-Fail}$. In general, for a given collector voltage bias (V_{C-Bias}) and load termination ($Z_L = R_L + jX_L$) the voltage-limited RF output power SOA boundary during linear, uncompressed operation can be expressed as

$$P_{Out-Fail-V} \approx \frac{1}{2}\left(\frac{V_{Fail} - V_{C-Bias}}{|Z_L|}\right)^2 R_L \tag{41}$$

If the dynamic output voltage swing reaches its lower limit at the knee voltage V_{Knee}, gain compression occurs and the output waveform becomes distorted, extending to higher collector voltage as power is further increased. Thus, V_{Knee} will limit the maximum RF output power the device can sustain before failing. An effective shift in the *dc* collector voltage bias is used as a simple approximation to account for overdrive with respect to V_{Knee}, with V_C in Equation 41 being replaced with

$$V_{C-eff} = \frac{V_{Fail} + V_{Knee}}{2}. \tag{42}$$

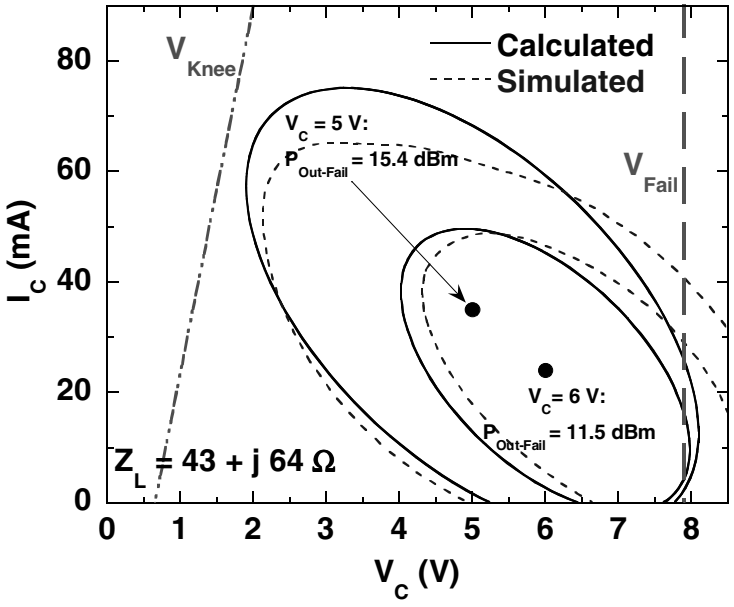

Figure 65: Calculated (solid lines) and simulated (dotted lines) dynamic load-lines at $P_{Out-Fail}$ for $Z_L = 43 + j64\ \Omega$ at $V_C = 5$ V and 6 V.

Thus,

$$P^*_{Out-Fail-V} \approx \frac{1}{8}\left(\frac{V_{Fail} - V_{Knee}}{|Z_L|}\right)^2 R_L \tag{43}$$

in the overdriven case where the lower side of dynamic voltage swing (V_{min}) reaches V_{Knee} but the upper side is still less than V_{Fail}. If V_{Knee} were constant, then it it clear from Equation 43 that $P^*_{Out-Fail}$ would be independent of collector bias voltage. However, V_{Knee} will increase with collector current (I_{Knee}) according to the relation

$$V_{Knee} = I_{Knee}R_{Sat} + V_{ON}. \tag{44}$$

Here, R_{Sat} represents the slope of the bipolar I-V characteristic in the saturation region and V_{ON} represents the saturated collector voltage where $I_C = 0$. Both these terms can be readily obtained from the transistor output characteristics. The minimum of the dynamic voltage swing can be represented in terms of the *dc* bias point, load impedance, and maximum dynamic current swing ($I_{Out-Peak}$):

$$V_{min} = V_{C-Bias} - |Z_L|(I_{Out-Peak} - I_{C-Bias}). \tag{45}$$

During compressed operation, it is assumed that V_{min} and $I_{Out-Peak}$ are equal to V_{Knee} and I_{Knee}, respectively. Thus, setting Equations 44 and 45 equal to one another and solving for V_{Knee} will yield

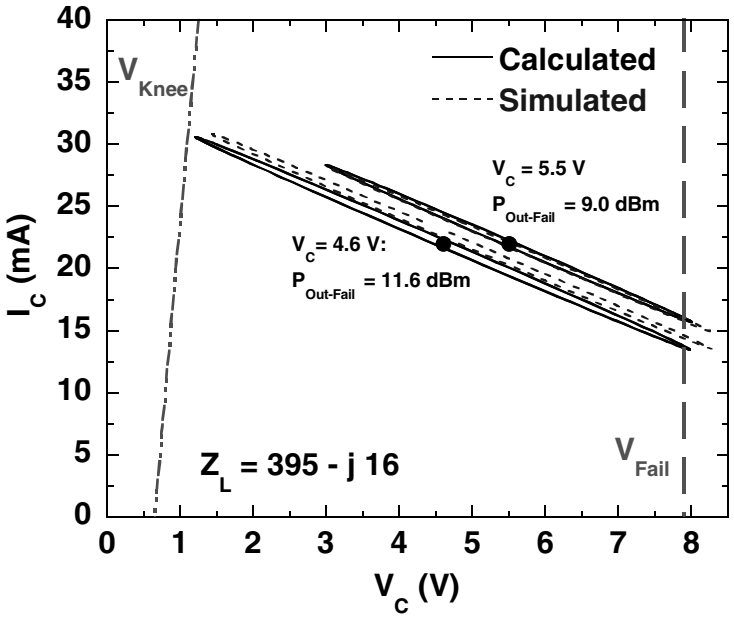

Figure 66: Calculated (solid lines) and simulated (dotted lines) dynamic load-lines at $P_{Out-Fail}$ for $Z_L = 395 - j16\ \Omega$ at $V_C = 4.6$ V and 5.5 V.

an expression for V_{Knee} to be used in Equation 43:

$$V_{Knee} = \frac{R_{Sat}(V_{C-Bias} + |Z_L|I_{C-Bias}) + |Z_L|V_{ON}}{R_{Sat} + |Z_L|}. \tag{46}$$

Figure 67 shows the measured $P_{Out-Fail}$ results obtained at different collector voltage bias for two load impedances. The measured data shows that V_C and Z_L both significantly influence the dynamic SOA of the cascode core, and that this boundary can be accurately predicted by Equations 41 and 43, with V_{Fail} set to 8.15 V ($\chi = 0.075$). Measurements on the 4x power cores (with Q1 and Q2 each having a total device area of 0.12x18x4 μm^2) confirm the geometrical independence predicted for the voltage-limited dynamic SOA. The region where the role of V_{Knee} and gain compression become important is indicated by the flattening of $P_{Out-Fail}$ at lower V_C. For comparison, the dashed curve in Figure 67 shows the value predicted when the effects of V_{Knee} are not accounted for. The Matlab code developed to calculate the voltage-limited RF failure limit is provided in Appendix A1.

Figure 68 shows experimental and calculated $P_{Out-Fail}$ contours across Z_L for the cascode power core at $V_C = 5$ V. The calculated results were obtained from Equation 41 for the same conditions used in Figure 67 ($V_{Fail} = 8.15$ V, $\chi = 0.075$). This result shows that for practical load

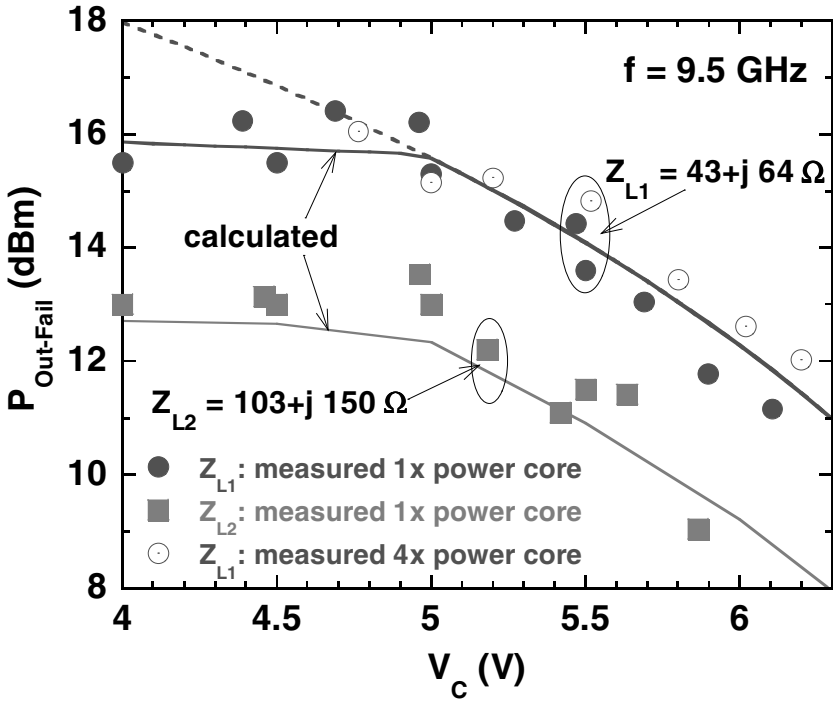

Figure 67: Measured (markers) and calculated (lines) cascode voltage-limited output power failure thresholds as a function of V_C for different load impedances.

impedances near the optimal gain match condition, the dynamic SOA threshold is typically voltage limited and generally decreases as $|Z_L|$ becomes larger, as predicted in Equations 41 and 43. However, for lower impedances ($|Z_L|^2/R_L < 100\ \Omega$), the experimental results for $P_{Out-Fail}$ are lower than predicted for the given V_{Fail}, indicating that in this region the dynamic SOA is primarily limited by the current swing at the output of the SiGe HBT rather than the output voltage swing.

4.5.4 Current-Limited Dynamic SOA Results

In addition to the dynamic voltage limits, transistor failure can also occur when the dynamic output current swing ($I_{Out-Peak}$) exceeds the safe-operating limit I_{Fail} during large-signal RF operation, particularly for collector voltage bias exceeding V_{C-crit} because of the high localized current densities associated with strong pinch-in [20]. This failure condition is shown in Figure 69, which shows the dynamic current and voltage swings calculated based on failure limits measured at $V_C = 5$ V for increasing R_L. For $R_L = 395\ \Omega$, device failure occurs at 10.6 dBm due to the maximum dynamic voltage limit V_{Fail}. However, for lower load resistances the failure point occurs at considerably

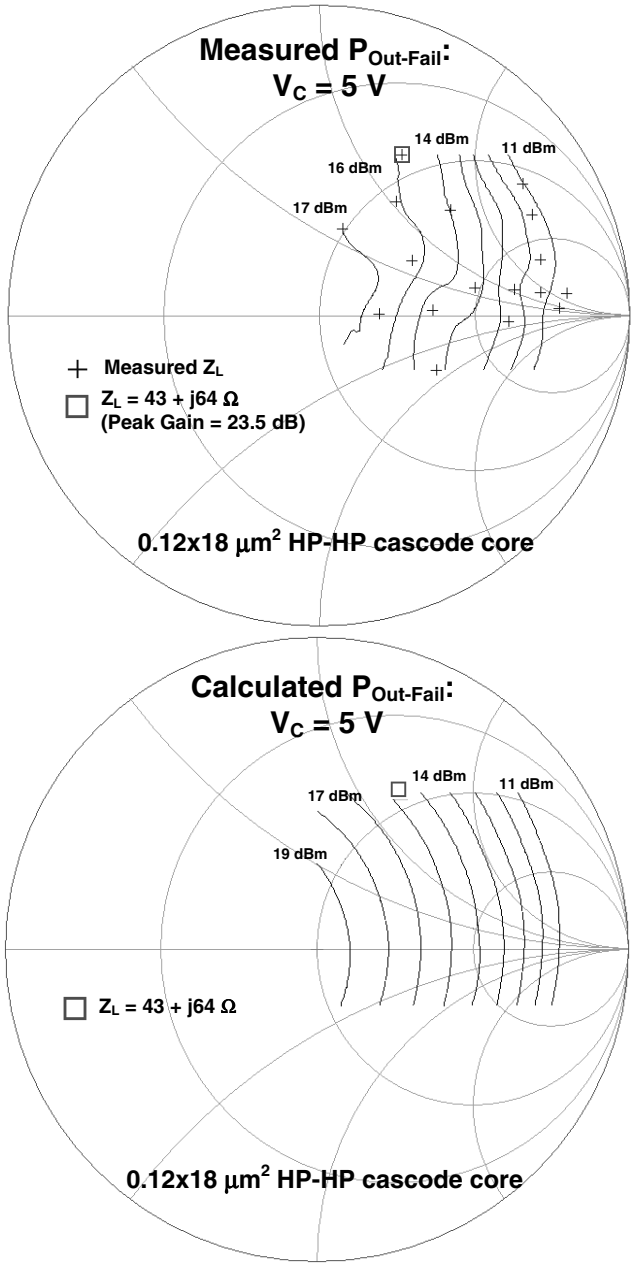

Figure 68: Measured (top graph) and calculated (bottom graph) 1-dBm contours of voltage-limited $P_{Out-Fail}$ across load impedance for $V_C = 5$ V at 9.5 GHz. $Z_o = 50\ \Omega$.

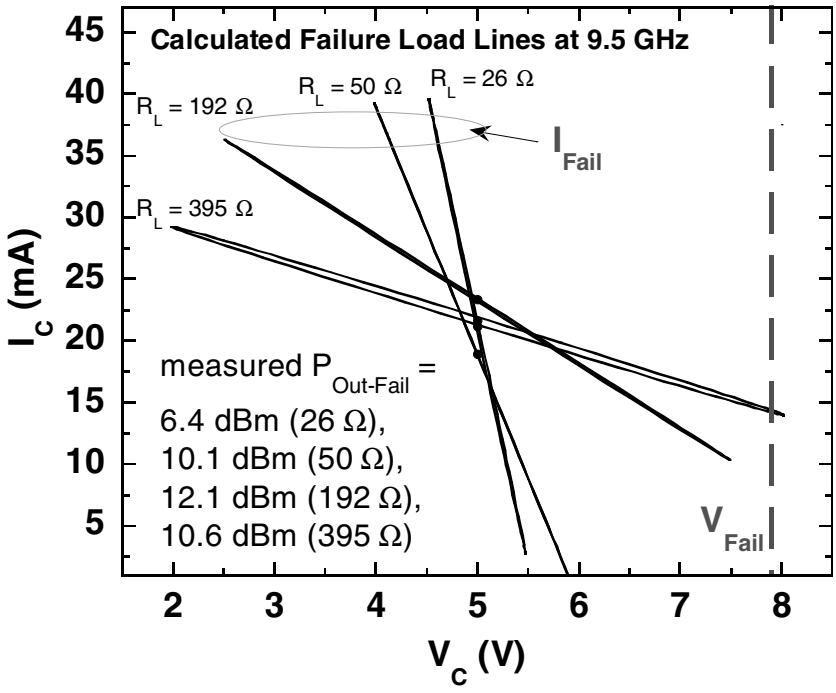

Figure 69: Calculated dynamic load-lines at $V_C = 5$ V based on experimental $P_{Out-Fail}$ results for different load impedance conditions.

lower output voltage swing. In these cases the large-signal SOA is considered to be limited by the dynamic output current swing and not the output voltage.

For operating conditions where the *dc* collector current (I_{C-Bias}) does not depend strongly on the input power drive (such as Class A operation), the condition dictating the current-limited RF output power SOA boundary can be expressed as

$$P_{Out-Fail-I} \approx \frac{1}{2} \left(I_{Fail} - I_{C-Bias}\right)^2 R_L. \tag{47}$$

This relation shows that if either collector bias current is increased or load resistance decreased, device failure because of the maximum current SOA will occur at lower RF power. For conditions where the collector current bias depends strongly on input power drive (such as Class AB operation) and $I_{C-Bias} = I_{Out-Peak}/2$, this RF SOA limit is simply

$$P^*_{Out-Fail-I} \approx \frac{1}{8} I^2_{Fail} R_L. \tag{48}$$

Figure 70 shows the measured and calculated $P_{Out-Fail}$ SOA boundary for the SiGe HBT cascode power amplifier core. For $Z_L = 50\ \Omega$ the large-signal RF SOA is clearly current-limited and

decreases for larger bias current. The maximum current limit I_{Fail} = 37.5 mA used for the calculation is consistent with the *dc* operating limits observed from independent measurements on the same SiGe HBT cascode structure under similar bias conditions [65]. Unlike the voltage operating limits, which are well predicted by BV_{CBO} and do not depend on device geometry, the maximum current limits are more difficult to predict and can depend strongly on device geometry and trajectory of the output loadline. Moreover, pinch-in effects can play a significant role in lowering this current limit, as is shown in Figure 71. Here the measured *dc* collector currents (which increase with RF power because of device self-bias) at the onset of device failure are plotted for different collector voltages. The pinch-in limit V_{C-crit} for the SiGe HBT cascode is also plotted. From this plot it is apparent that devices operating in the pinch-in region fail at excessive RF power (P_{in} near -5 dBm) in the manner described above, with $P_{Out-Fail}$ around 10 dBm. Interestingly, for V_C bias below V_{C-crit}, the cascode can sustain much larger RF power (P_{in} greater than 10 dBm), with the output power saturating above 15 dBm without the device failing. This result indicates that the I_{Fail} limit is considerably lower (below 40 mA, compared to above 150 mA) when the transistor is operated within the pinch-in region. Clearly this pinch-in threshold plays an important role in the dynamic safe-operating area boundary for cascode SiGe HBTs and should be carefully considered for designs operating under large-signal conditions.

4.5.5 Guidelines for Reliable Large-Signal Operation

As demonstrated in Section 4.3, operating the cascode SiGe HBT power core at higher collector voltage bias can result in higher P1dB and saturated output power. However, considering the dynamic SOA limits it becomes clear that the goals of achieving maximum output power performance and ensuring maximum device reliability can conflict with one another. Therefore, several guidelines are recommended to guarantee safe large-signal operation.

For a given bias condition it is clear that the output power should always remain less than $P_{Out-Fail}$, as expressed in Equations 41, 43, 47, and 48. Therefore, for RF gain G, the maximum input power driving the cascode amplifier stage should be less than $P_{Out-Fail} - G$. In certain cases it may not be feasible to control the input power to the amplifier. Therefore, as a guideline, one should ensure the device is biased such that it enters into RF gain compression prior to $P_{Out-Fail}$.

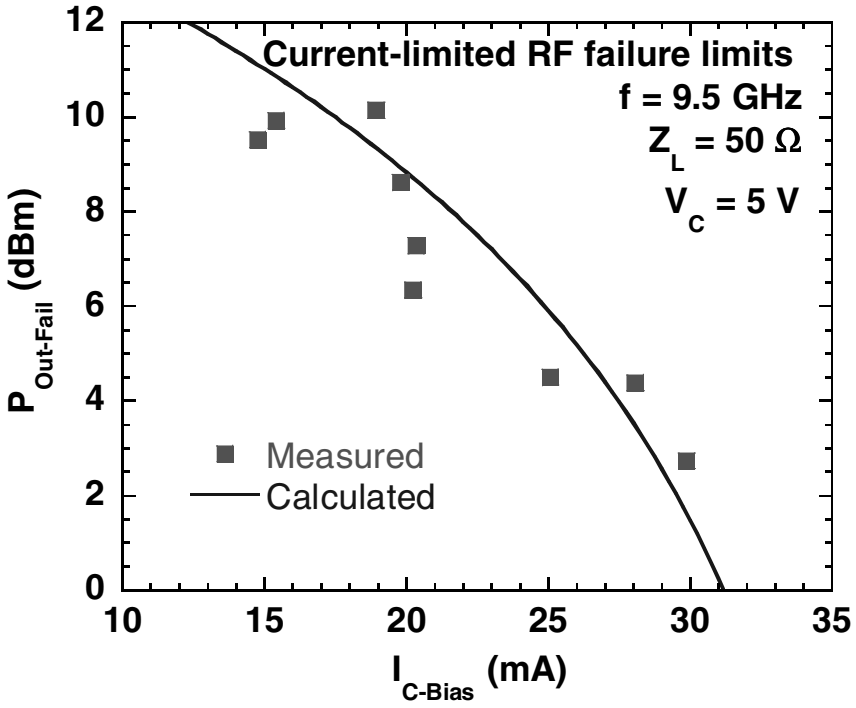

Figure 70: Measured (markers) and calculated using Equation 47 (lines) cascode output power failure threshold as a function of *dc* collector current bias for the current-limited case at $Z_L = 50\ \Omega$.

It is clear from Figure 67 that $P_{Out-Fail}$ is relatively flat for compressed operation at lower V_C. However, for uncompressed (linear) high-power operation at high V_C, $P_{Out-Fail}$ degrades rapidly as V_C increases. This transition occurs for the condition $P^*_{Out-Fail-V} = P_{Out-Fail-V}$, which is satisfied when $V_C = (V_{Fail} + V_{Knee})/2$. Therefore, it is recommended that the collector bias voltage be lower than this transition point in order to maximize both power performance and dynamic SOA. In the most conservative case, maximum dynamic reliability can be achieved at the expense of RF power performance by lowering the V_C bias such that the saturated output power (P_{sat}) is less than $P_{Out-Fail}$. This will ensure (assuming the Z_L remains constant) that the dynamic output voltage swing will never exceed the limit V_{Fail}, regardless of input power drive to the PA.

In order to avoid failures associated with the dynamic current limits, the collector voltage bias should be lower than the pinch-in voltage (V_{C-crit}) since the I_{Fail} limits (and consequently $P_{Out-Fail-I}$) are reduced considerably when the device is biased above this threshold. In addition, the effects of dynamic stress, as discussed in Section 4.4, should also be considered with respect to long-term PA reliability and operating lifetime [65].

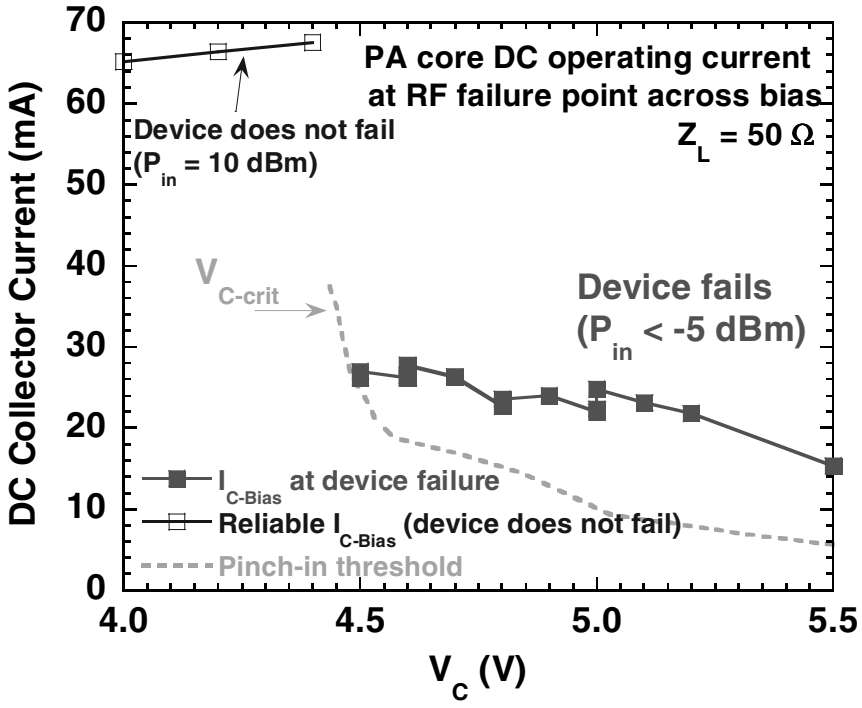

Figure 71: Measured cascode output power failure threshold as a function of *dc* collector voltage bias for the current-limited case at $Z_L = 50\ \Omega$.

As with any reliability degradation mechanism, the statistical variations associated with large-signal RF SOA should be considered carefully. Figures 72 and 73 show the measured $P_{Out-Fail}$ distributions of the voltage-limited and current-limited RF failure limits for sample sizes of 50 devices and 23 devices, respectively. The failure limit (x-axis) is compared to the calculated RF failure limit (normalized to 0 dB), and the results below 0 dB indicate the measured RF failures that occurred at lower power than predicted by calculation. For voltage-limited RF failures, these results in Figure 72 indicate that the majority of failures occur within ± 0.5 dB of the predicted RF power, although occasional failure was observed up to 2 dB lower than predicted. The standard deviation for the voltage-limited case was approximately 0.7 dB. The standard deviation for the current-limited RF failures in Figure 73 was considerably larger (1.2 dB). A broader scattering for current-limited RF failures is expected due to the wider variability observed for the I_{Fail} limit compared to V_{Fail}.

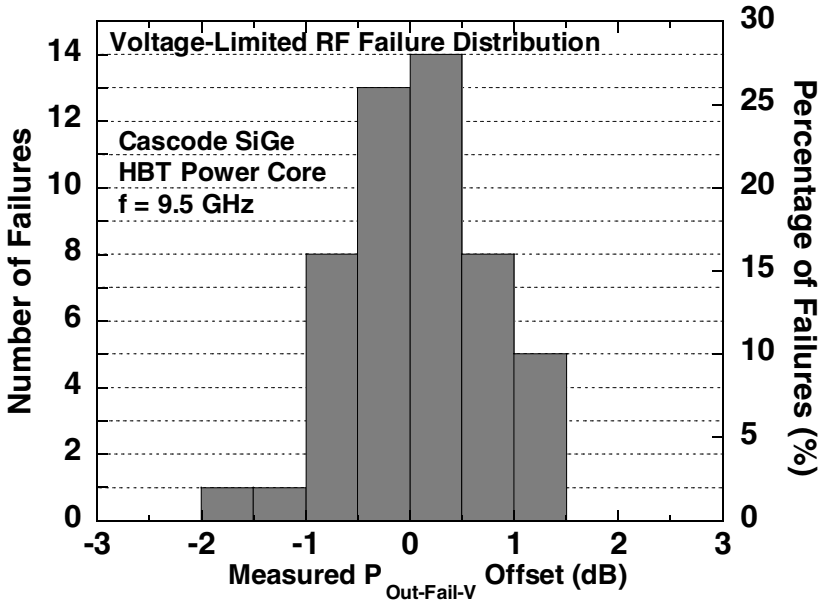

Figure 72: Statistical distribution of experimental $P_{Out-Fail}$ data for voltage-limited RF failures of the SiGe HBT cascode power cores, with respect to the calculated failure limit. The 0.5-dB sorting bins on the x-axis represent *measured* $P_{Out-Fail-V}$[dBm] minus *calculated* $P_{Out-Fail-V}$[dBm].

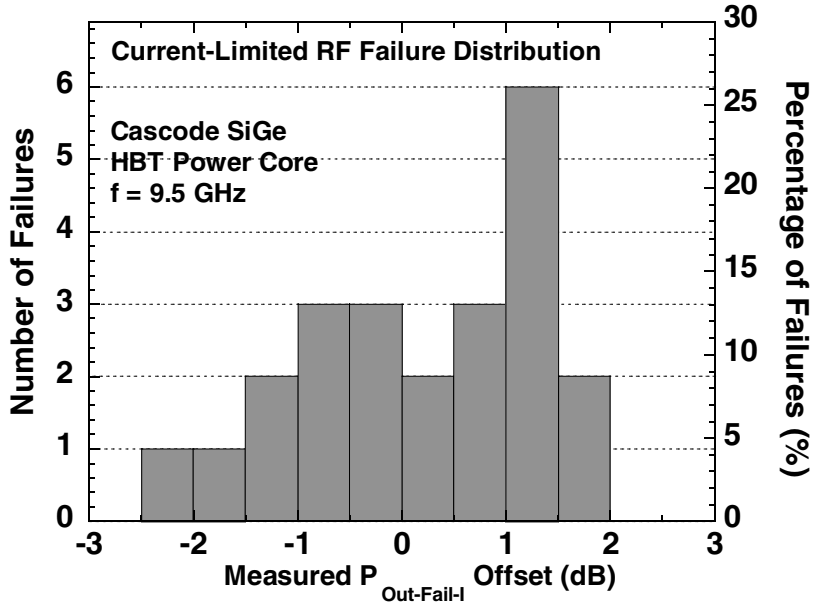

Figure 73: Statistical distribution of experimental $P_{Out-Fail}$ data for current-limited RF failures of the SiGe HBT cascode power cores, with respect to the calculated failure limit. The 0.5-dB sorting bins on the x-axis represent *measured* $P_{Out-Fail-I}$[dBm] minus *calculated* $P_{Out-Fail-I}$[dBm].

CHAPTER V

INTERMODULATION DISTORTION IN SIGE HBTS

5.1 Introduction

Achieving high dynamic range (DR) is a very broad topic with a variety of tuning knobs at both the device and circuit-level [14],[66],[67]. For the proposed research, understanding the key transistor-level limits and trade-offs for distortion characteristics is considered to be a logical starting point for improving the DR performance at the device, circuit, and system levels.

Numerous factors at the device-level play a role in determining the linearity of a SiGe HBT, including bias, device geometry, frequency of operation, and impedance termination. In particular, a broad understanding of the linearity behavior across both bias and geometry must be realized before one can make truly informed comparisons of DR between different devices, technology nodes, or transistor technologies. For example, Figure 74 shows IIP3 as a function of collector current density (J_C) for a SiGe HBT biased at different collector voltages (V_{CB}). Clearly, J_C plays a strong role in linearity, resulting in almost 20 dBm of variation in IIP3. At high bias (near J_C at peak f_T), increasing V_{CB} from 0 to 1.5 V increases IIP3 by over 10 dB. Understanding the bias dependence of individual distortion contributions is essential for both device optimization and linear circuit design. Linearity in the common-base (CB) configuration is of interest because it applies to numerous practical RF circuit topologies used in blocks such as mixers and cascode amplifiers, and can withstand higher collector voltages for applications requiring more output power [24], [68].

In this chapter, two-tone measurements and harmonic balance simulations are utilized to examine these complex linearity dependencies in SiGe HBTs. When well understood, the observed variations across bias and geometry may be leveraged for optimized circuit design, and an example looking at a cascode amplifier stage is presented. Also, the intermodulation distortion during CB operation is examined experimentally and analytically using Volterra series. Simple new expressions for individual nonlinear contributions are presented that accurately predict linearity across bias and provide greater intuitive understanding of the role of various device parameters on CB linearity.

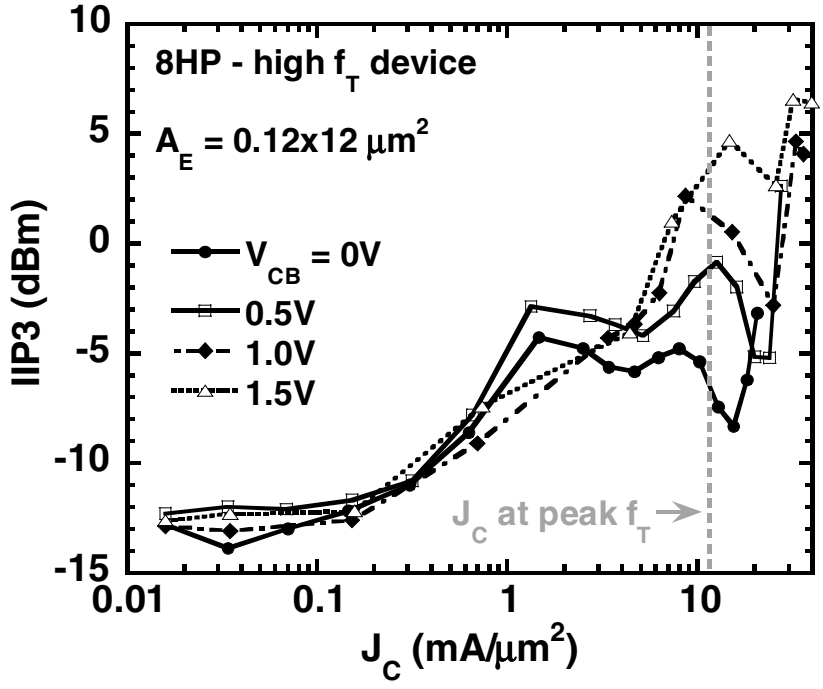

Figure 74: IIP3 as function of collector current density at different collector voltages for a 200 GHz SiGe HBT. Two-tone measurements were taken at 9.5 GHz with 100 MHz tone spacing.

5.2 Dynamic Range Tensor Analysis

5.2.1 Role of Device Bias and Geometry on Linearity

For the proposed research, the dynamic range tensor (DR tensor) was developed and used to examine linearity across a broad range of geometry and bias conditions. Here IIP3, Gain, and *dc* power are characterized at a fixed frequency across bias (J_C and V_{CB}) for different device geometries. Noise figure (NF) represents another important transistor characteristic with bias and geometry dependencies. For brevity, NF analysis in the DR tensor is not included here. To demonstrate the DR tensor, Figure 75 shows contours of constant IIP3 across J_C and V_{CE}, representing a "slice" of the DR tensor at a particular device geometry (A_E). Contours for other transistor characteristics, such as *dc* power, exist in the same space, as the graphic to the right of Figure 75 illustrates.

Using analysis software such as MATLAB, this broad set of data (IIP3, gain, *dc* power, SOA, NF) can be represented as overlapping tensors within the three-dimensional space (J_C, V_C, and A_E). The data contained within the DR tensor can then "flattened" in a variety of ways to probe the various trade-offs associated with linearity performance. The algorithm developed for the proposed

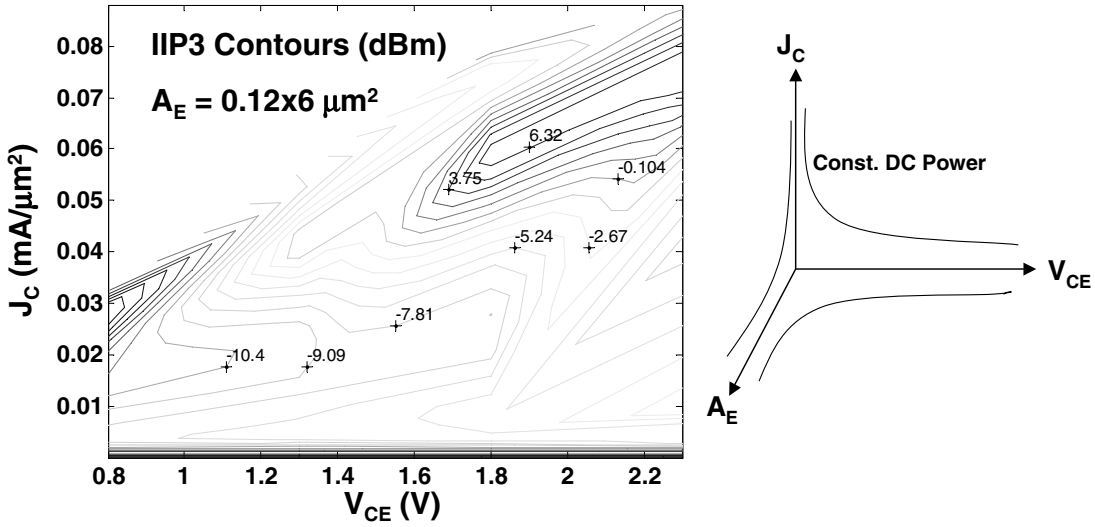

Figure 75: Common-emitter (CE) IIP3 contours across collector current density and collector voltage for a third-generation high performance (HS) SiGe HBT. Right: graphic representation of the dynamic range (DR) tensor, with contours of constant *dc* power indicated.

research is as follows: for a parameter of interest (*i.e.* *dc* power, gain, or NF), a desired range of values ($a_0 \leq a_n \leq a_N$) are swept. For each value (a_n), the condition (tensor index) of maximum IIP3 that exists on that contour is determined. Thus, the DR tensor analysis serves to locate and identify only the *optimal* (maximum) linearity performance for the device based on a specified set of criteria.

For example, the DR tensor can be analyzed with respect to *dc* power. This is shown in Figure 76, where the results for different device geometries are shown as separate curves. From this characteristic, the optimal device sizing and bias for maximum linearity can be chosen for a given *dc* power requirement. For instance, the point indicated in Figure 76 shows that for $P_{dc} = 0.65$ mW, a maximum IIP3 of -3.4 dBm can be obtaining using 0.12x3 μm^2 device biased at $J_C = 2.25$ mA/μm^2 and $V_{CE} = 0.8$ V. The corresponding power gain under these conditions is 9.7 dB.

The relationship between linearity and the various device bias and geometry conditions is quite complex in nature. However, several general trends are observed:

1. IP3 tends to increase with J_C, and often reaches a local maxima near J_{Kirk}.

2. At low injection, IP3 is not strongly affected by V_{CB}. At medium and high injection, linearity

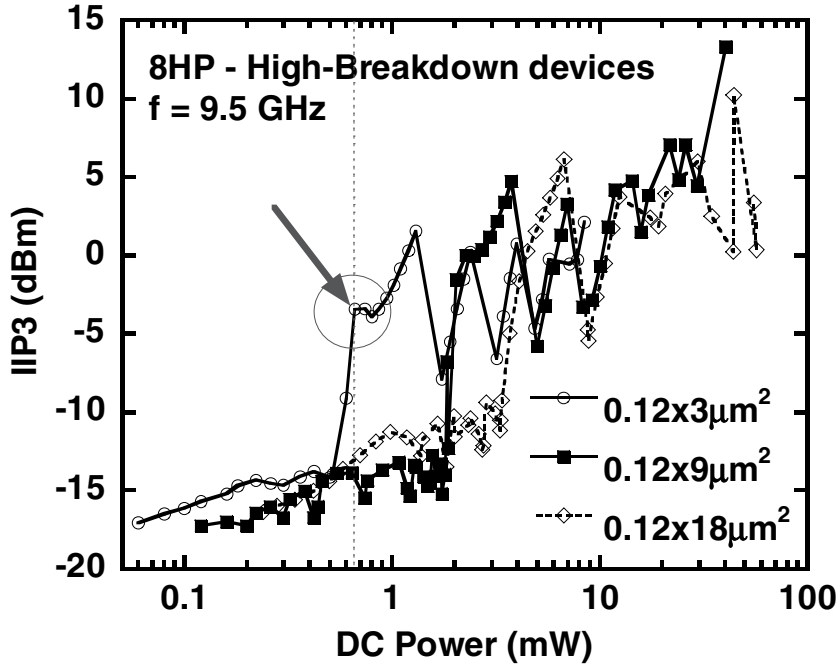

Figure 76: Peak IIP3 extracted as a function of DC power from the DR tensor for a SiGe HBT in CE configuration.

tends to increase with V_{CB} because of increasing C_{CB}, although IP3 eventually decreases at high V_{CB} due to avalanche nonlinearities.

3. IP3 tends to increase with A_E, because of increased "back-off" (smaller v_{be} with respect to V_T for given i_c).

Note that the product of J_C, A_E, and V_C determines the *dc* power dissipation (P_{dc}). Altogether, IP3 tends to increase with P_{dc}, as indicated in Figure 76.

5.2.2 Application of the Dynamic Range Tensor

This section demonstrates the application of the DR tensor for the design an cascode amplifier stage for maximum IIP3 and OIP3. As indicated by Equation 5, the final in a series of cascaded gain stages typically will have the greatest impact on IIP3. However, initial two-tone simulations and measurements for 50 Ω load impedance indicate that much higher linearity is available for CB configurations compared to CE. So, assuming linearity is limited by input (CE) stage, the proposed cascode design approach is as follows:

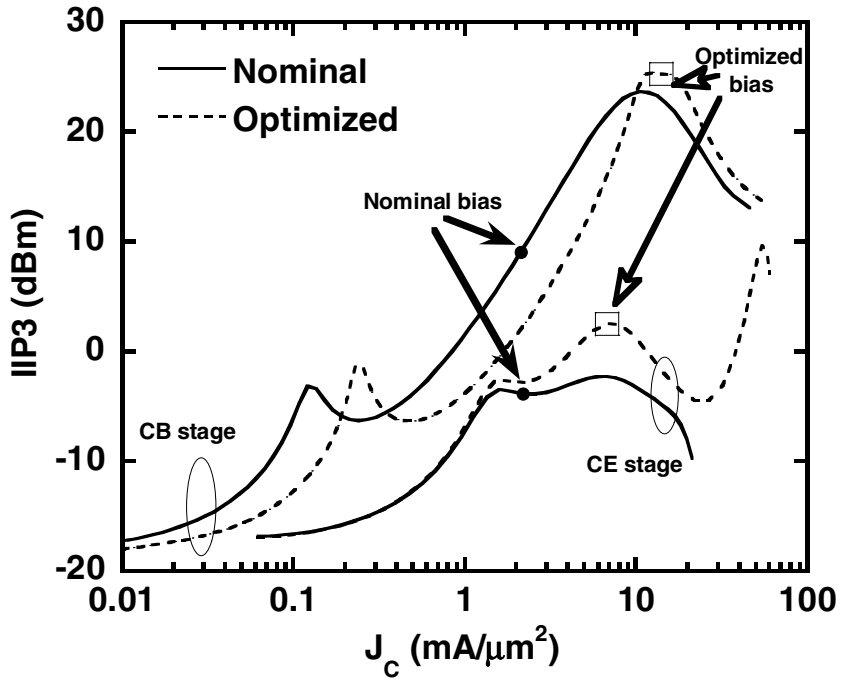

Figure 77: Simulated common-emitter (CE) and common-base (CB) IIP3 characteristics across collector current density comparing nominal and optimized (high linearity) cases.

1. Perform DR tensor analysis of CE transistor to select optimal device size and bias for linearity, given gain, power dissipation, and NF requirements.

2. Perform DR tensor analysis of CB transistor to determine optimal voltage bias and collector current density. Total current, and sizing of CB transistor, is thus determined by the I_C required in the CE transistor.

Following this methodology, a cascode amplifier stage in 200 GHz SiGe HBT technology was optimized for linearity. The DR tensor data and circuit performance results were obtained using the harmonic balance simulator in Agilent ADS. For comparison, a nominal case is examined along side the optimized case. When the DR tensor analysis is performed for the input (CE) transistor in the cascode pair, the optimal size (0.12x18 μm^2) and bias (V_{CB} = 1.0 V, J_C = 6.8 mA/μm2) were chosen to provide maximum linearity (IIP3 = 2.5 dBm) with adequate gain (21 dB). For the output (CB) transistor, the optimal bias was determined to be V_{CB} = 1.5 V, J_C = 14 mA/μm2. As a result, an emitter area of 0.12x9 μm^2 was selected.

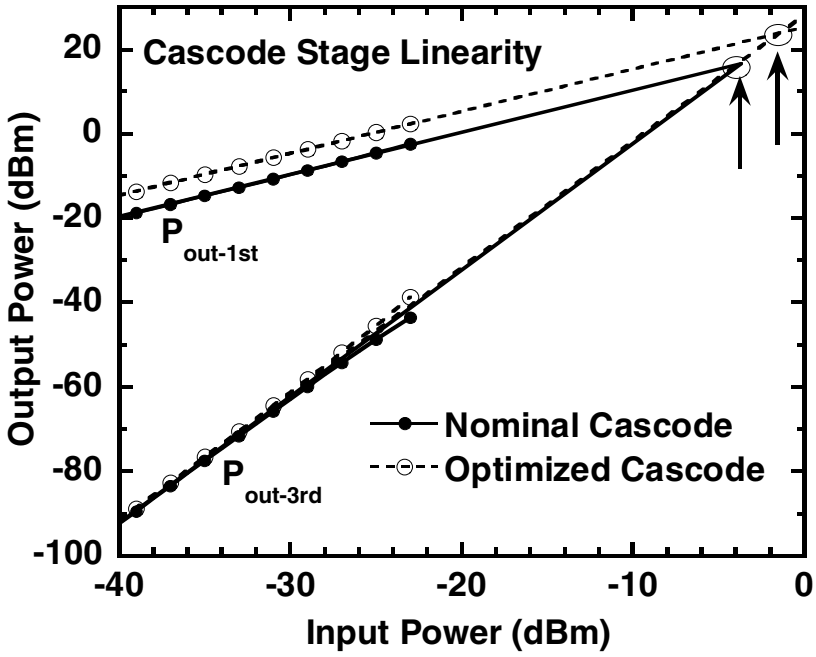

Figure 78: Simulated fundamental ($P_{o-1^{st}}$) and third-order intermodulation product ($P_{o-3^{rd}}$) versus input power for the nominal and optimized (high linearity) cascode stages.

The CE and CB linearity for the nominal and optimized cases are compared across J_C in Figure 77. The respective bias points are indicated. Figure 78 shows the linearity performance for the nominal and optimized cascode stages. For the optimized design, the fundamental ($P_{out-1st}$) improves without increasing the intermodulation ($P_{out-3rd}$), resulting in a 6.2 and 7.2 dB increase in IIP3 and OIP3, respectively. The design parameters and performance results for the nominal and optimized cascode stages are summarized in Table 6. As shown, this improvement in IP3 occurs with a small (1 dB) improvement in gain and a five-fold penalty in *dc* power dissipation.

For this brief analysis, the effects of source and load impedance on linearity have been neglected. However, the impedance conditions, particularly at the load, can influence the magnitude of the second and third harmonics, which will effect the intermodulation characteristics [67]. For CB operation, the influence of load termination has been reported to be particularly strong, with significant degradation to linearity observed for impedance matched conditions [68]. This is an important concern for high dynamic range performance, and is examined experimentally in Section 5.3 and analytically using Volterra series in Section 5.4.

Table 6: Comparison of nominal and optimized cascode stage designs and performance results.

	Nominal	Optimized
A_{E-top} (μm^2)	0.12x18	0.12x18
V_{C-top} (V)	2.5	4.3
V_{B-top} (V)	1.8	2.8
$A_{E-bottom}$ (μm^2)	0.12x18	0.12x9
$V_{B-bottom}$ (V)	0.85	0.875
IIP3 (dBm)	-3.7	2.5
OIP3 (dBm)	16.5	23.7
P_{dc} (mW)	11.9	62.8

5.3 Common-Base Intermodulation Distortion in Advanced SiGe HBTs

5.3.1 Motivation

The common-base (CB) configuration applies to numerous practical circuit topologies used in RF blocks such as mixers and cascode amplifiers. Therefore, understanding the CB intermodulation distortion of SiGe HBTs is of practical interest for designs requiring high dynamic range. A previous study showed CB linearity to be considerably more sensitive to changes in the load match (Z_L) compared to CE linearity [68]. However, that analysis was limited to a single bias point, and it has been shown that wide variations in third-order intercept (IP3) can be observed as a function of device bias. Therefore, examining the linearity behavior across bias is essential for an accurate and broad analysis of transistor linearity performance, both in terms of physical understanding at the device level and for designing circuits with high dynamic range.

This study investigates CB linearity characteristics across bias in third-generation (200 GHz) SiGe HBT technology [57]. The respective roles of bias current, collector voltage, geometry, load match, and collector design are examined comprehensively. Comparisons between measured data and harmonic balance simulations are presented. Additional insight into CB linearity using Volterra series will be presented in Section 5.4.

In a CB configuration, a SiGe HBT can obtain substantially higher linearity than in CE mode [66]. This difference is demonstrated in the two-tone measurement results shown in Figure 79, which compares the fundamental output power ($P_{Out-1st}$) and third-order intermodulation product ($P_{Out-3rd}$) as a function of input power (P_{in}) for a SiGe HBT in CE and CB configurations at identical bias conditions. In CB mode, the power gain is considerably lower (11.4 dB compared to

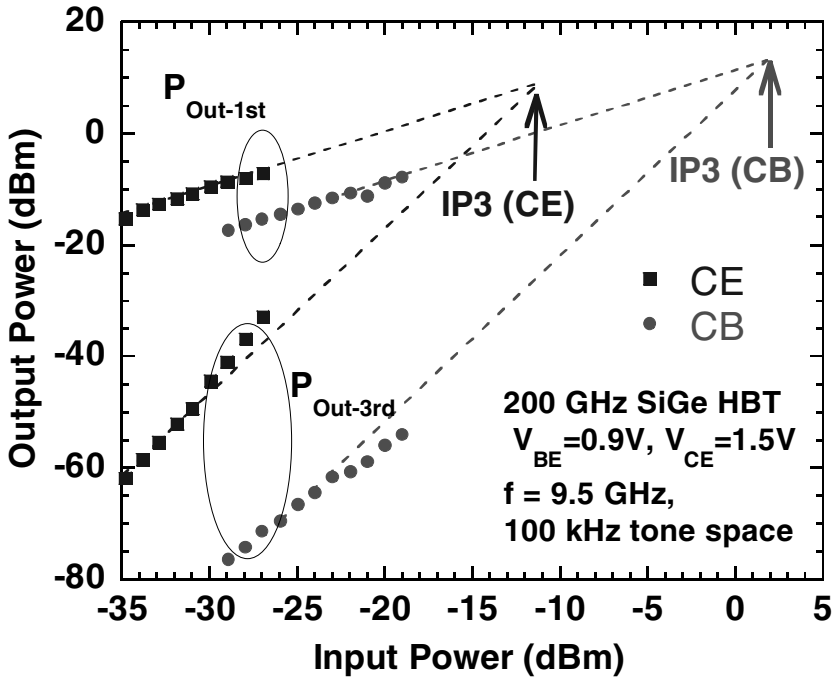

Figure 79: Fundamental ($P_{Out-1st}$) and third-order intermodulation ($P_{Out-3rd}$) for CE and CB configurations as a function of input power measured for a 0.12x3 μm^2 SiGe HBT.

20.5 dB). However, IMD3 (the ratio of $P_{Out-3rd}$ to $P_{Out-1st}$ in dBc) is considerably lower for the CB configuration. This results in substantial improvement in linearity, and is reflected in increases to both IIP3 and OIP3.

This superior linearity performance during CB operation is observed across a wide bias range, as shown in Figure 80. Here, IIP3 is compared across I_C for identical devices in CE and CB configurations. Analysis in [69] concludes that the linearity improvement for the CB configuration is primarily because of the higher input current drive (and thus higher P_{in}) associated with a given IMD3.

5.3.2 Experimental Setup

The experimental setup for this study used a Maury load pull system with impedance tuners at the source and load of the DUT. An Agilent 4155 was connected to bias tees at the input and output of the DUT to supply the *dc* bias. For the RF input, tones from two signal generators were combined using a hybrid power combiner. A spectrum analyzer at the output was used to measure the

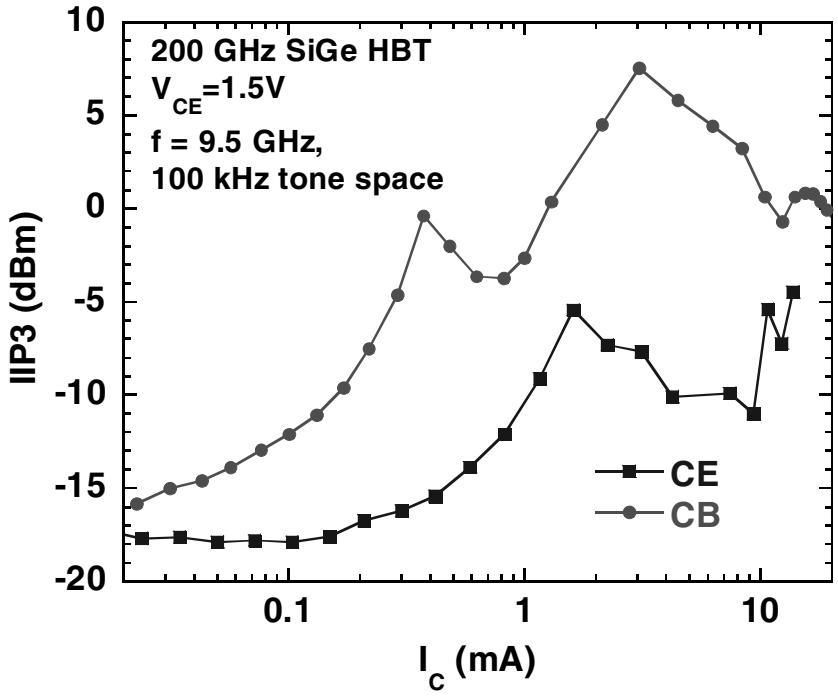

Figure 80: Comparison of measured CE and CB linearity across bias for a 0.12x3 μm^2 SiGe HBT.

fundamental and intermodulation output power. Automated bias and power sweeps were performed using the Maury ATS300 software, which controls the tuners, signal generators, *dc* bias, and takes output readings from the spectrum analyzer. The two-tone measurements were performed at 9.5 GHz at 100 kHz tone spacing. For its broadband response, and to maintain generality across bias, the nominal source and load terminations (Z_S and Z_L) were set to 50 Ω.

Several experiments were performed on third-generation SiGe HBTs [57] to examine the various influences on CB linearity. Two-tone measurements using 50 Ω source and load terminations were performed across I_C at fixed V_{CB} (1.5 V) on various device geometries (0.12x3 μm^2, 0.12x12 μm^2, and 0.12x18 μm^2) on the standard-breakdown transistor. Next, load pull measurements were performed to tune the load impedance (Z_L) for maximum (uncompressed) gain at V_{BE} = 0.9 V and V_{CB} = 1.5 V on several different device geometries, and the two-tone measurements were repeated to examine the role of output match on IP3.

Additional measurements were performed to examine the role of collector voltage bias and collector design on linearity. For this experiment a device size of 0.12x3 μm^2 was used and Z_L was matched for maximum gain at V_{BE} = 0.9 V, V_{CB} = 1.5 V. Two-tone measurements were taken

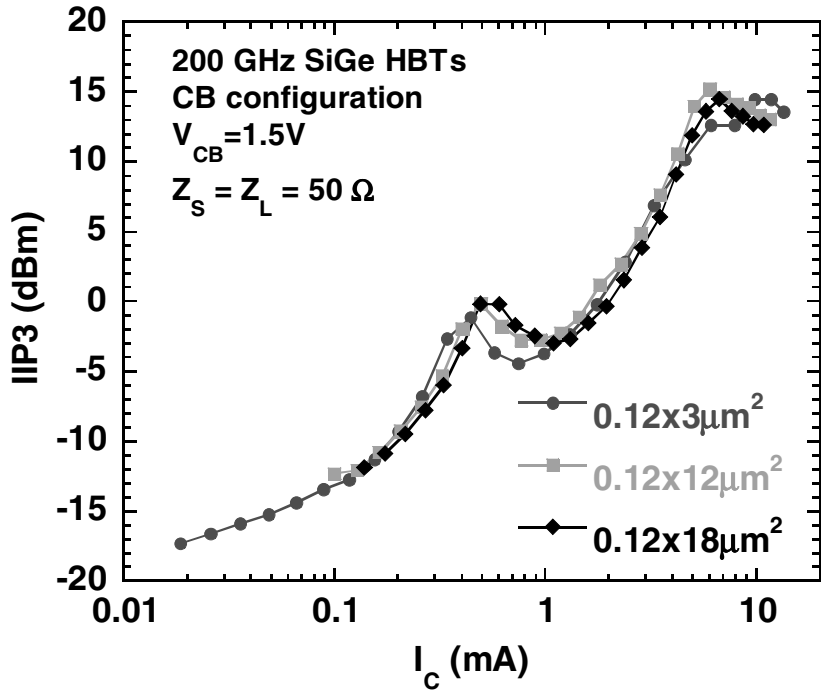

Figure 81: Measured CB IIP3 as a function of I_C for SiGe HBTs with three different geometries. Z_L is 50 Ω.

across I_C at various values of V_{CB} (from 0.1 V to 2 V) on the standard-breakdown (HS), medium-breakdown (MB) and high-breakdown (HB) devices.

5.3.3 Role of Geometry and Load

Figure 81 shows the IIP3 in the CB configuration as a function of I_C bias as emitter length (L_E) is increased from 3 to 18 μm. In this bias range, IIP3 is observed to be largely independent of device geometry. This indicates that g_m, which (to first order) is geometry independent at low-injection, represents the dominant device nonlinearity at low and moderate I_C bias during CB operation [70]. At higher I_C, the CB configuration shows an impressive linearity performance, with IIP3 reaching 15 dBm and OIP3 approaching 20 dBm for the unmatched (50 Ω) case.

Figure 82 shows the fundamental (9.5 GHz) load-impedance planes for two different emitter lengths in the CB configuration. OIP3 contours (1 dB each) are shown and the optimal load impedance for gain matching (minimum output reflection) is indicated. For $L_E = 3$ μm and $L_E = 18$ μm (not shown), Z_L for maximum gain is significantly different than Z_L for maximum linearity.

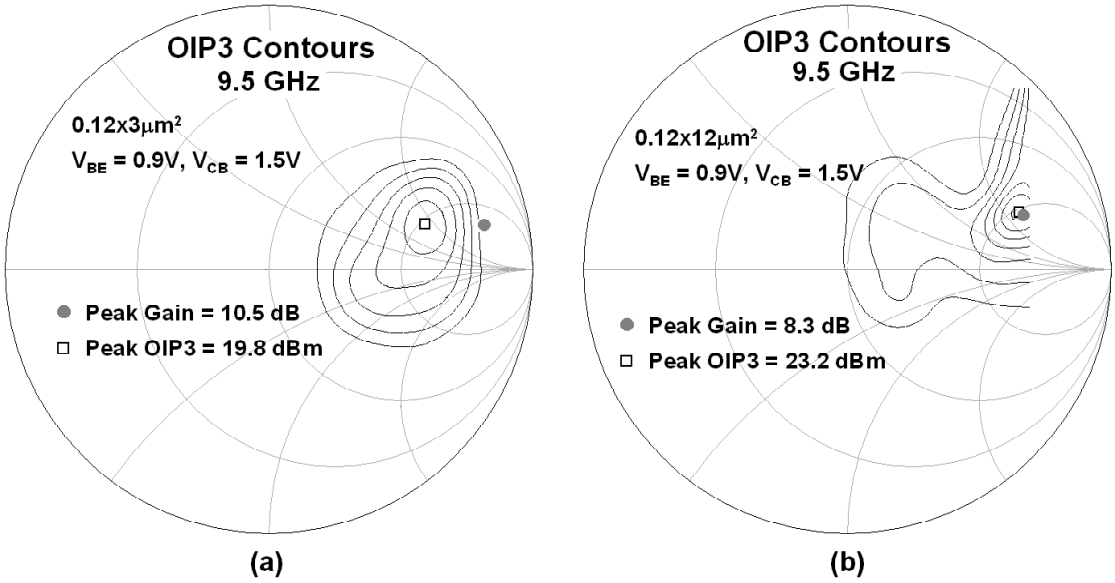

Figure 82: Measured CB load match for peak gain (filled circles) and peak OIP3 (open squares) for SiGe HBTs with different geometries: (a) 0.12x3 μm^2, and (b) 0.12x12 μm^2. 1 dB contours for OIP3 are shown.

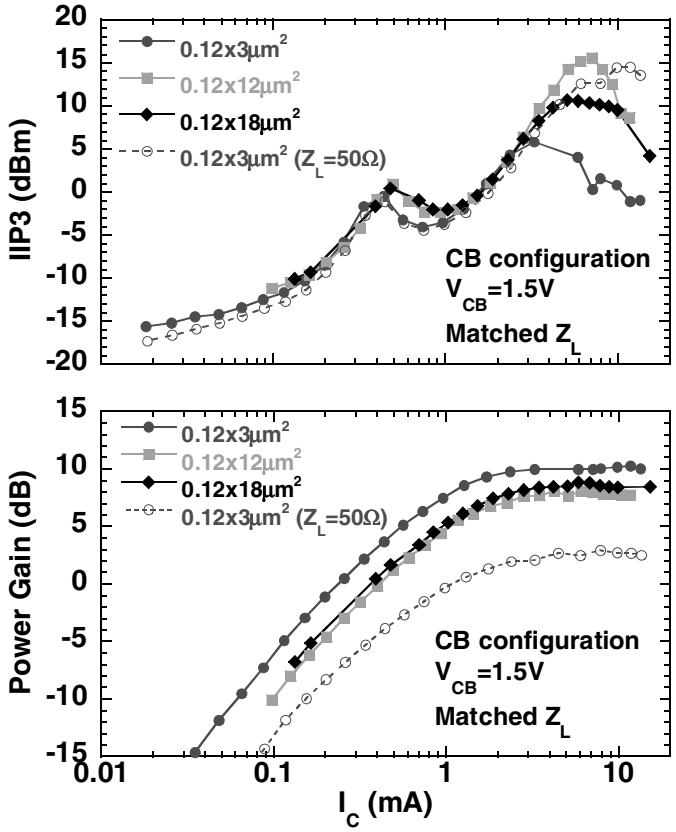

Figure 83: CB IIP3 (top) and gain (bottom) as a function of I_C measured for SiGe HBTs with three different geometries. Z_L is matched for gain. IIP3 for Z_L = 50 Ω on 0.12x3 μm^2 is shown for comparison.

However, the 0.12x12 μm^2 device, when load-matched for power gain, shows near optimal linearity.

Figure 83 shows the linearity and power gain across I_C for the SiGe HBTs with the output impedance matched for maximum gain. For L_E = 3 μm, the linearity and gain results for Z_L at 50 Ω are plotted once again for comparison, showing that power gain increases by as much at 7 dB with the tuned output match. At the same time, with L_E = 3 μm the peak IIP3 for the matched case is degraded by nearly 10 dB compared to the 50 Ω load. At I_C below 3 mA, no significant change in IIP3 is observed as for matched Z_L. At higher I_C, however, matching Z_L results in considerable degradation in IIP3 in all cases except the 0.12x12 μm device. Therefore, by tuning the interaction between CB linearity and gain with respect to load impedance, device geometry can play a significant role in the design of well-matched RF blocks with high linearity.

5.3.4 Role of Collector Bias and Collector Design

Figure 84 shows CB linearity across I_C for different V_{CB} for the HS, MB, and HB SiGe HBTs. For reference, the position of I_C at peak f_T is indicated for each. At low currents, neither collector voltage nor collector design show any significant influence on IIP3. However, at higher I_C the collector voltage plays a strong role in the linearity for all three cases, with IIP3 tending to increase with increasing V_{CB}. This increase is attributed to a variation in the onset of base-pushout (Kirk effect), since changing V_{CB} changes the position of the collector-base depletion region with respect to the collector doping profile.

As expected, the I_C-threshold (dotted vertical lines in Figure 84), below which IIP3 is independent of V_{CB}, decreases with I_C at peak f_T as collector doping is reduced. In the HS SiGe HBT, the high-current peak in IIP3 (around 2 mA) increases with V_{CB} from 0 V to 1 V. For the MB device, the minimum value of IIP3 that occurs near 1 mA rises significantly as V_{CB} increases to 1.5 V. For the HB device, the magnitude and position of the low-current local IIP3 maxima shifts upward considerably as V_{CB} is increased to 2 V. This behavior is observed in the HB device because the "high-current" linearity degradation occurs at nearly the same I_C as the "low-current" g_m peak, leading to a complex interaction between the two linearity influences.

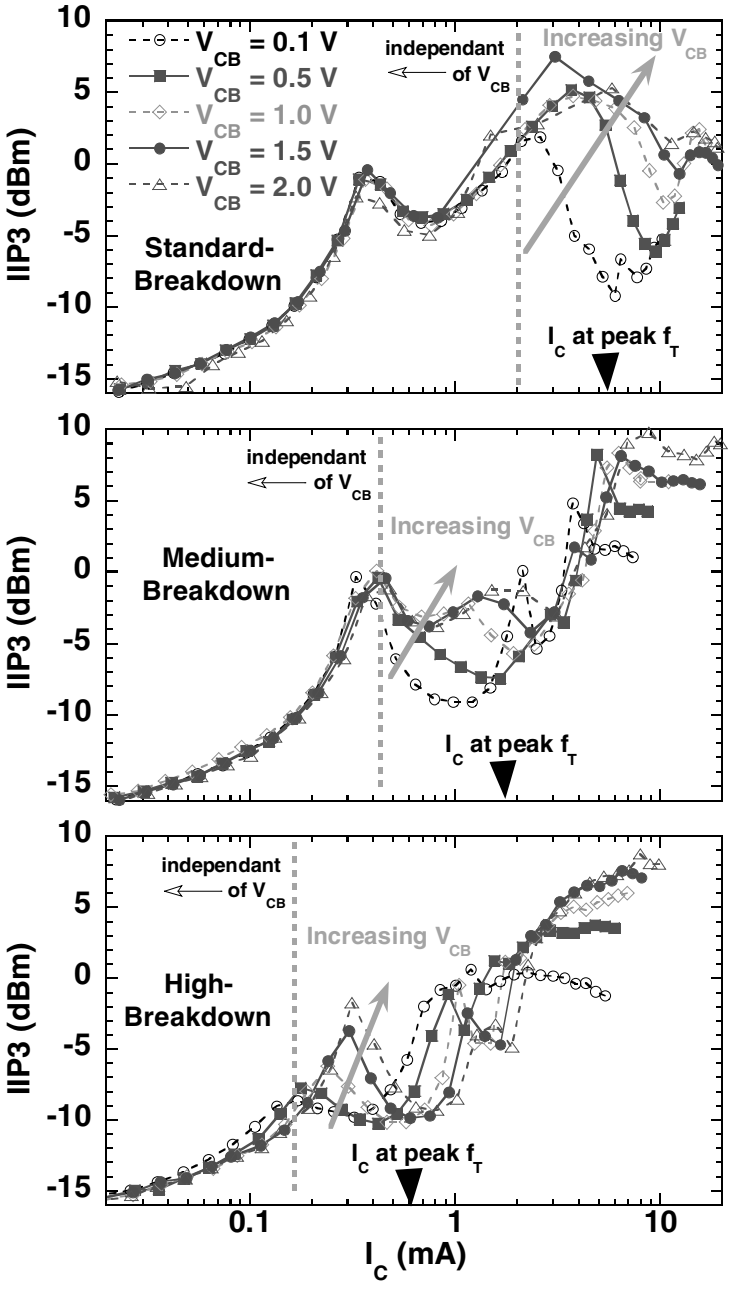

Figure 84: Measured CB IIP3 as a function of I_C at different V_{CB} for SiGe HBTs (A_E = 0.12x3 μm^2) with different collector designs: (top graph) HS with high collector doping, (middle graph) MB with medium collector doping, and (bottom graph) HB with low collector doping.

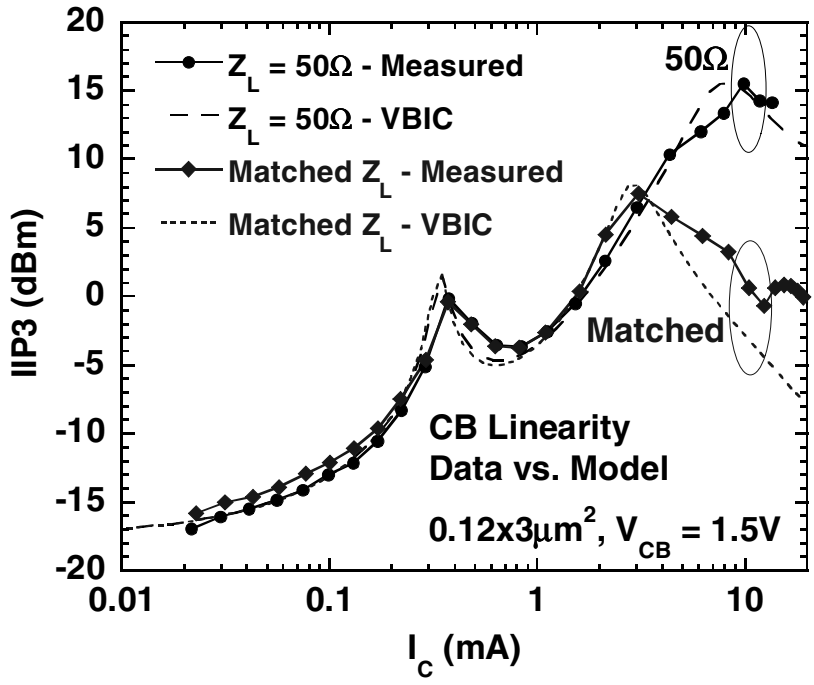

Figure 85: Data and model (VBIC) comparison of CB IIP3 under 50 Ω and matched load conditions.

5.3.5 Data and Model Comparison

Figure 85 compares the measured and modeled IIP3 across bias for the 0.12x3 μm^2 HS device in CB configuration. Both the 50 Ω and matched-load cases are shown. The simulated data was obtained using the harmonic balance engine in ADS with the standard VBIC model from the design kit developed for this SiGe HBT BiCMOS technology.

Good agreement is observed between the measured and simulated IIP3 data, with the VBIC model capturing the position and magnitude of the low-current local maxima and the drop in IIP3 at high I_C. The linearity degradation associated with the impedance match is also captured in simulation, although at high current the model predicts a faster roll-off of IIP3 with I_C than is observed in measurement. Additional simulations were performed at different V_{CB} and compared to the measured data for both the standard- and high-breakdown devices, confirming that the overall linearity behavior was well-predicted by the VBIC model. However, it should be noted that at higher I_C (>1 mA) the high-breakdown model shows IIP3 to be significantly higher than measured.

5.4 Volterra Series Analysis of Common-Base Nonlinearities

5.4.1 Background and General Approach

For additional insight into the various nonlinearity contributions that determine the intermodulation distortion for the SiGe HBT in common-base (CB) operation, analysis using Volterra series was performed. As a general mathematical technique for solving systems of nonlinear equations as higher-order perturbations to a linearized system, the Volterra series method is appropriate for analyzing and modeling weak nonlinearities that occur in active devices (e.g., SiGe HBTs) under small-signal operating conditions [1].

For example, collector current in a bipolar device is a nonlinear (exponential) function of base-emitter voltage, or

$$I_C = I_S exp\left(\frac{qV_{BE}}{kT}\right). \tag{49}$$

This results in a nonlinear transconductance ($g_{m,eff}$), which may be described by a series expansion of the *ac* current-voltage expression:

$$i_c(t) = K_{1g_m} v_{be}(t) + K_{2g_m} v_{be}^2(t) + K_{3g_m} v_{be}^2(t) + ..., \tag{50}$$

with the coefficients describing the $I-V$ nonlinearity generally expressed as

$$K_{ng_m} = \frac{1}{n!} \left.\frac{\partial^n f(v_{be})}{\partial v_{be}^n}\right|_{v_{be}=V_{BE}}. \tag{51}$$

Thus, the nonlinear transconductance coefficients can be written for the ideal exponential device as

$$K_{1g_m} = g_m = \frac{qI_C}{kT}, \tag{52}$$

$$K_{2g_m} = \frac{1}{2!}\frac{q^2 I_C}{(kT)^2}, \tag{53}$$

$$K_{3g_m} = \frac{1}{3!}\frac{q^3 I_C}{(kT)^3}, \tag{54}$$

and so on, although the first three terms of the expansion are typically sufficient given the assumption of weak nonlinear (small-signal) operation [1]. For real devices, which may deviate from the ideal exponential relationship, these coefficients may be extracted directly from experimental $I-V$ data.

In this manner, the coefficients for all physical nonlinear contributions to the system may be determined. Using these coefficients, virtual current sources (I_{NL2-}, I_{NL3-}), which represent the

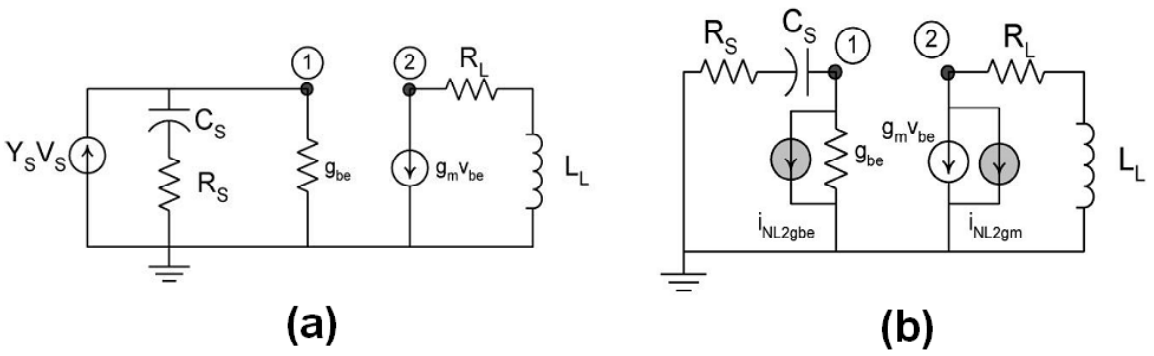

Figure 86: Simplified network for solving the (a) first-order and (b) second-order transfer functions for the common-emitter (CE) SiGe HBT amplifier [1]. The network for the third-order transfer functions is the same as (b), with the second-order nonlinear virtual current sources I_{NL2-g_m} and $I_{NL2-g_{be}}$ being replaced by the third order virtual sources: I_{NL3-g_m} and $I_{NL3-g_{be}}$, respectively.

higher-order nonlinear excitations, can be determined. The virtual current sources act as higher-order perturbations to the first-order (linearized) transfer function, as illustrated in Figure 86 for g_m and g_{be} ($= 1/r_\pi = g_m/\beta$) nonlinearities.

For this analysis of frequency-dependent CB nonlinearities, four dominant nonlinearity contributions are considered: the I_{CE} (or g_m) nonlinearity, the I_{BE} (or g_{be}) nonlinearity, and the nonlinear collector-base and base-emitter capacitances (C_{bc} and C_{be}, respectively). The networks used to solve the first-, second-, and third-order transfer functions in the CB configuration are presented in Figure 87. For simplicity, avalanche nonlinearities are not considered because of their minimal role at lower V_{CB}. Therefore, the approach presented here is considered valid for $V_{CE} < BV_{CEO}$, although this additional avalanche contribution may be considered in order to obtain greater accuracy at higher V_C.

The goals of this study are

1. Develop Volterra series kernels that capture common-base linearity performance (IIP3) for SiGe HBTs across collector current bias.

2. Analyze and determine dominant nonlinearity contributions during common-base operation and understand how these contributions vary across bias.

3. Obtain simplified expressions for common-base IIP3 based on Volterra series analysis that are useful for predicting linearity performance.

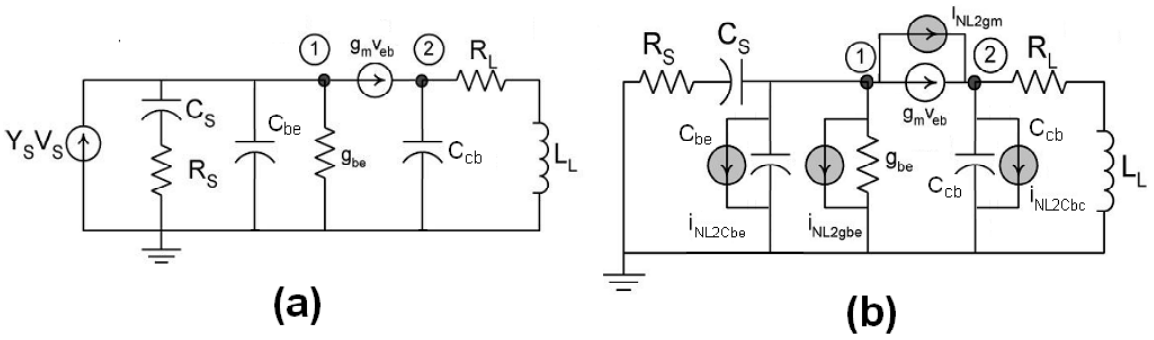

Figure 87: Simplified network used in this study for solving the (a) first-order and (b) second-order transfer functions for the common-base (CB) SiGe HBT amplifier. The network for the third-order transfer functions is the same as (b), with the second-order nonlinear virtual current sources being replaced by the third order virtual sources.

4. Gain understanding of the role of various device parameters- both external (such as source and load impedance) and internal (such as transconductance and nonlinear parasitic capacitance) on the linearity performance during common-base operation.

5.4.2 Results of Common-Base Volterra Series Calculation

Volterra series kernels for the SiGe HBT in the CB configuration were developed in Matlab. These functions were written to read in an input file that contains a vector of V_{BE} and I_C values across the bias range of interest, and corresponding tables of the necessary first-, second-, and third-order parameters for the device being studied. These parameters include *dc* current gain (β), g_m, K_{2g_m}, K_{3g_m}, g_{be}, $K_{2g_{be}}$, $K_{3g_{be}}$, C_{be}, $K_{2C_{be}}$, $K_{3C_{be}}$, C_{bc}, $K_{2C_{bc}}$, and $K_{3C_{bc}}$. This input data can be extracted for a specific V_{CB} from a *dc* I-V (Gummel) measurement to determine the g_m and g_{be} terms and an *ac* s-parameter measurement across the same range of I_C to determine the C_{bc} and C_{be} terms. Because the C_{bc} nonlinearities depend on both I_C and V_{CB}, an additional s-parameter measurement across V_{CB} is required to determine the C-V relationship and generate depletion capacitance terms associated with C_{bc}. Careful extraction of all these parameters is required across bias, because any errors in the higher-order derivatives can significantly limit the accuracy of the IIP3 calculation. The Matlab code developed for this study (presented in Appendix A2) is adaptable so that the higher-order nonlinearity coefficients can be determined beforehand and read from a table, or they can be calculated at runtime as derivatives of the first-order terms with respect to V_{BE}.

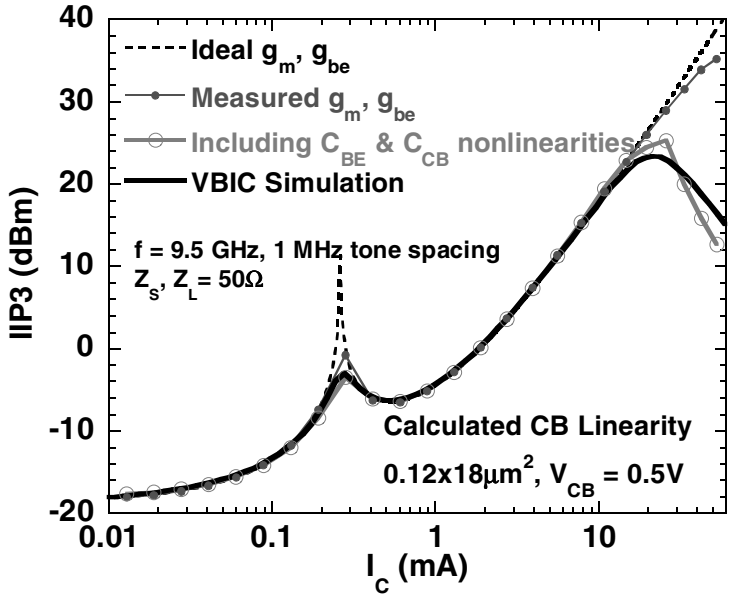

Figure 88: CB linearity calculated for various nonlinearity contributions for a 200 GHz SiGe HBT using Volterra series, compared with results from two-tone harmonic balance simulation of the VBIC model for the same device. $Z_L = 50\ \Omega$.

Figure 88 plots the CB IIP3 calculated for various nonlinearity contributions using Volterra series for a third-generation (200 GHz) SiGe HBT [57] compared with results from a two-tone harmonic balance simulation of the model for this device. Figure 88 shows close agreement between Volterra series and the "VBIC Simulation" across I_C. The CB linearity at low current is dominated by the exponential i_c - v_{be} dependence and is well-captured by "Ideal g_m, g_{be}" in Figure 88, which uses the linearity coefficients for an ideal exponential device (Equations 52 - 54). Since the "ideal" device does not consider high-injection effects, the IIP3 will continue to rise as I_C increases. Using measured (as opposed to ideal) g_m and g_{be} values and derivatives ("Measured g_m, g_{be}" in Figure 88) slightly shifts and dampens the strong nonlinearity cancellation peak at low I_C. However, neither case captures the degradation of IIP3 observed at high I_C. To capture this behavior, the capacitive nonlinear contributions must be accounted for, since C_{bc} and C_{be} become strongly nonlinear with the onset of base push-out (Kirk effect) at high injection.

The top graph of Figure 89 shows the various third-order nonlinear current sources (I_{NL3-g_m}, $I_{NL3-g_{be}}$, $I_{NL3-C_{bc}}$, and $I_{NL3-C_{be}}$) calculated for a SiGe HBT, compared across I_C with the corresponding IIP3 performance (in the bottom graph) calculated for the same device. As expected,

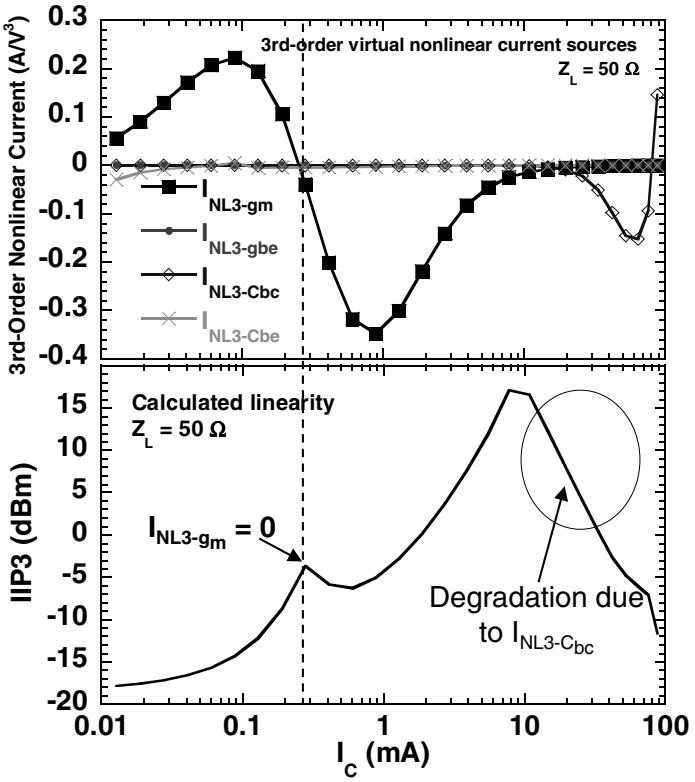

Figure 89: Top graph: third-order nonlinear current sources for various contributions across I_C for $Z_L = 50\ \Omega$, calculated using Volterra series of a SiGe HBT in the CB configuration. Bottom graph: corresponding CB IIP3 performance across bias.

the g_m nonlinearity is much larger than the other contributions at low I_C, and dominates the overall linearity performance. The low-current peak in IIP3 (near $I_C = 0.3$ mA) corresponds with a zero in the third-order g_m term as I_{NL3-g_m} crosses the x-axis. At higher I_C, the C_{bc} nonlinearity begins to play a dominant role in the overall linearity, causing IIP3 to degrade as a function of I_C as the magnitude of $I_{NL3-C_{bc}}$ increases.

Experimental results in the previous section showed that the load impedance (Z_L) can have a strong effect on CB linearity at high injection and degrade peak-linearity performance for matched load impedances. To better understand these results, the role of load impedance on the various CB nonlinearity contributions was studied using Volterra series. Figure 90 shows IIP3 computed for a SiGe HBT as R_L is increased from 25 Ω to 200 Ω. Volterra series computations predict that for larger R_L CB IIP3 will begin to degrade at a lower I_C, thus reducing the maximum IIP3 achievable at high bias. This result is consistent with trends observed experimentally. Examining the individual nonlinearity contributions, Figure 91 shows that the magnitude of $I_{NL3-C_{bc}}$ increases

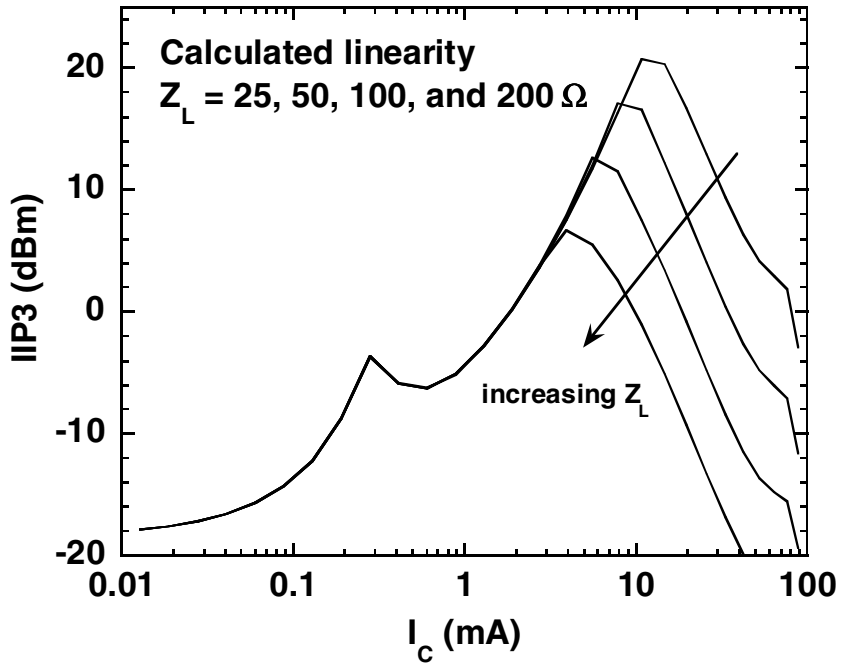

Figure 90: CB IIP3 performance across bias for a SiGe HBT calculated using Volterra series for different Z_L.

significantly when Z_L is increased, while the other nonlinearities are not affected. Since the magnitude of $I_{NL3-C_{bc}}$ tends to increase with I_C, this shift will result in $I_{NL3-C_{bc}}$ starting to dominate the overall device linearity at a lower value of I_C.

5.4.3 Simplified Expressions for Common-Base Nonlinearity

In general, IIP3 (in Watts) is proportional to the ratio of the first- and third-order transfer functions (H_{1o} and H_{3o}, respectively), and for a given source resistance (R_s) can be expressed as

$$\text{IIP3} = \frac{1}{6R_s}\frac{|H_{1o}(\omega_1)|}{|H_{3o}(\omega_1, \omega_2, \omega_3)|}, \tag{55}$$

evaluated at frequencies ω_1 (the fundamental), ω_2 (= ω_1+tone spacing), and ω_3 (= $-\omega_1$) [1]. Solving the first- and third-order transfer functions using the CB admittance matrix yields the expression

$$\text{IIP3} = \frac{|A|}{|6R_s^2(I_{NL3-g_m}(1-A) - (I_{NL3-g_{be}} + I_{NL3-C_{be}})A - I_{NL3-C_{bc}}|}, \tag{56}$$

for $A = g_m/Y_{in}(\omega_1)$ and $Y_{in}(\omega) = 1/R_s + g_{be} + g_m + j\omega C_{be}$. Increasing the magnitude the dominant nonlinear current source in the denominator will tend to decrease IIP3 as the overall nonlinearity

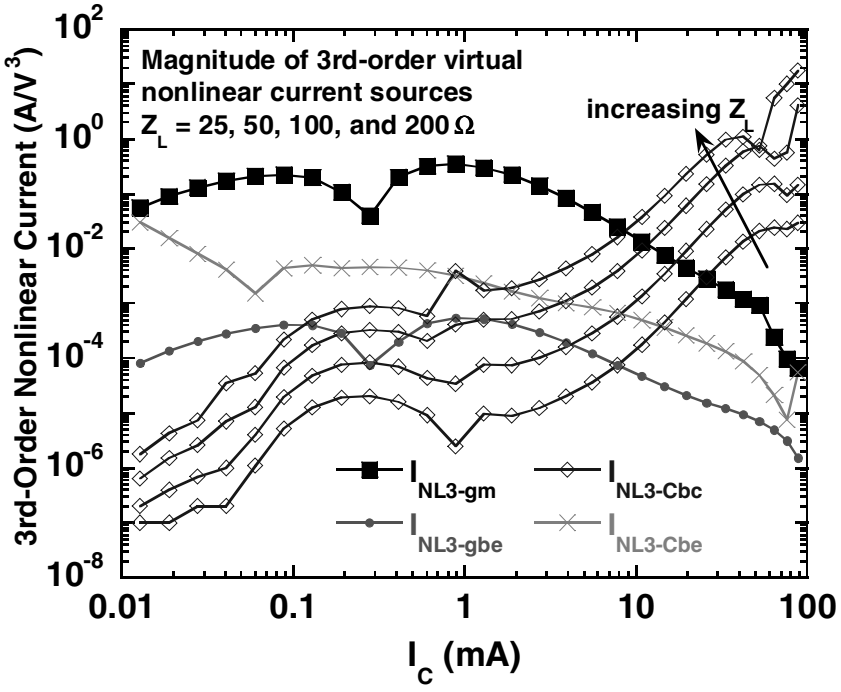

Figure 91: Virtual current sources calculated with Volterra series for a CB SiGe HBT for various Z_L. Only $I_{NL3-C_{bc}}$ shows any change as Z_L is increased.

is increased. Based on Volterra series calculations, expressions for the nonlinearity current sources were determined. These expressions were carefully reduced to eliminate negligible terms, and simplified using the assumption $\omega_1 \approx \omega_2$. From this, the transconductance nonlinearity can be written as

$$I_{NL3-g_m} \approx \frac{1}{B}\left[K_{3g_m} - \frac{2}{3}K_{2g_m}^2\left(\frac{2}{Y_{in}(0)} + \frac{1}{Y_{in}(2\omega_1)}\right)\right], \tag{57}$$

for $B = R_s^3 Y_{in}(\omega_1)^2 Y_{in}(-\omega_1)$. This expression shows that I_{NL3-g_m} will depend strongly on both the second- and third-order g_m nonlinearity terms, and its magnitude will tend to decrease as Y_{in} increases with g_m. In a similar fashion, the C_{bc} virtual nonlinear current can be written as

$$I_{NL3-C_{bc}} \approx \frac{-j\omega_1 K_{3C_{bc}}}{B}\frac{(g_m Z_L)^3}{1 + j\omega_1 C_{bc} Z_L}. \tag{58}$$

This expression indicates that the $I_{NL3-C_{bc}}$ is proportional to the third-order C_{bc} nonlinearity term, and its magnitude will increase in a cubic fashion as Z_L increases. Figure 92 compares the results of the new simplified calculations of I_{NL3-g_m} and $I_{NL3-C_{bc}}$ for a common-base SiGe HBT with the

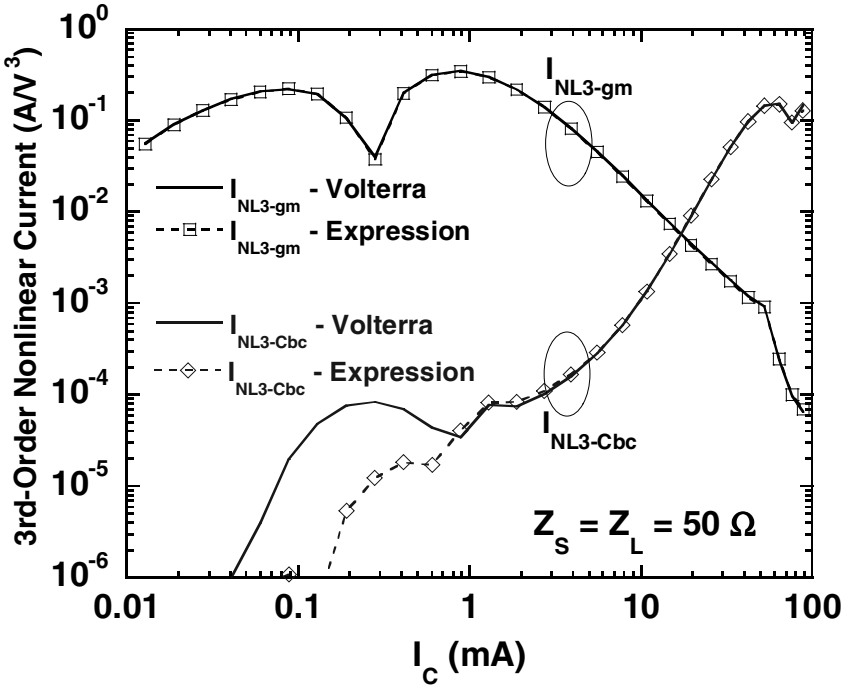

Figure 92: Virtual current sources for nonlinear g_m and C_{bc} of a CB SiGe HBT comparing the full Volterra computation with direct calculations. "I_{NL3-g_m} - Expression" plots Equation 57 while "$I_{NL3-C_{bc}}$ - Expression" plots Equation 58.

results computed using Volterra series, showing a very close match between the methods of calculation. For I_{NL3-g_m}, the direct expression of Equation 57 plotted in Figure 92 matches almost exactly with the Volterra series computation. Beyond low currents, the direct expression for $I_{NL3-C_{bc}}$ given by Equation 58 matches almost exactly with the Volterra series calculation. The discrepancy at low current should not affect the overall IIP3 calculation since such small values of $I_{NL3-C_{bc}}$ have no observable influence on linearity in this region. Thus, the bias, frequency, and load dependance of the dominate CB nonlinearities are accurately captured using very simple expressions.

The analysis of the individual nonlinearity contributions, as illustrated in Figures 89 and 91, indicates that the overall linearity in the CB configuration is dominated at low-current by g_m and at high-current by C_{bc}, and that g_{be} and C_{be} play only a minor role in CB linearity. Therefore, to simplify the overall expression these terms are left out, or

$$I_{NL3-g_{be}} \approx 0, \tag{59}$$

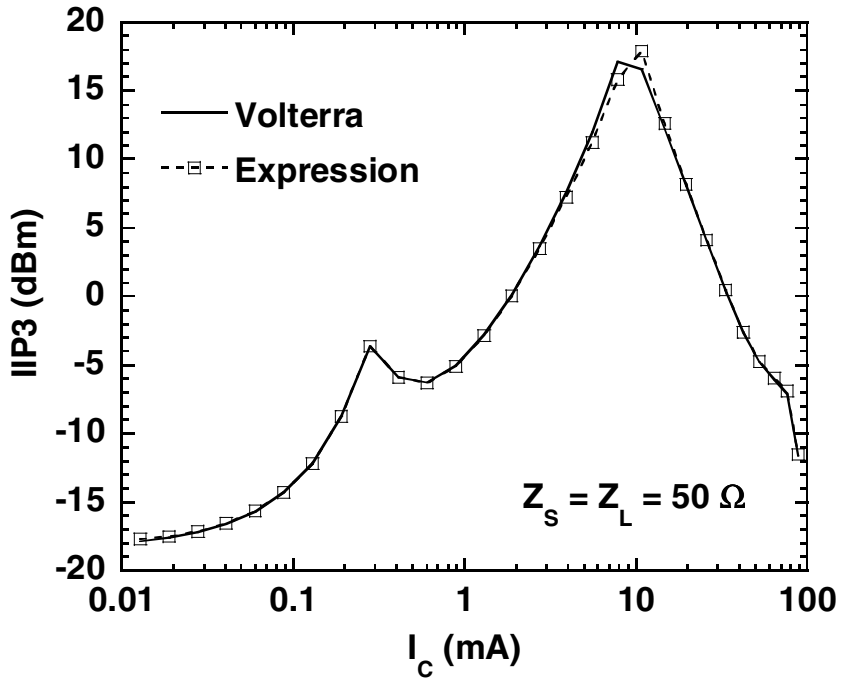

Figure 93: CB IIP3 for a SiGe HBT, comparing the full Volterra computation with direct calculations using Equations 56 - 60.

and

$$I_{NL3-C_{be}} \approx 0. \tag{60}$$

Figure 93 shows the direct calculation of IIP_3 across bias (using Equations 56 - 60) compared with Volterra series computations. The simple calculations agree closely with Volterra series results, and neglecting the C_{be} and g_{be} nonlinear terms shows no appreciable loss in accuracy for CB linearity.

The peak that occurs in IIP3 at low-current is a distinctive and fundamental feature of CB linearity that can be analytically examined as a function of I_C using the expression for I_{NL3-g_m} in Equation 57. Neglecting frequency effects associated with C_{be}, the condition for $I_{NL3-g_m} = 0$ can be simply expressed as

$$K_{3g_m} = \frac{2K_{2g_m}^2}{Y_{in}(0)} \tag{61}$$

By replacing g_m, K_{2g_m}, and K_{3g_m} with the respective expression for an ideal exponential device (as given in Equations 52-54) and solving for I_C, one finds the bias condition for this low-current IIP3

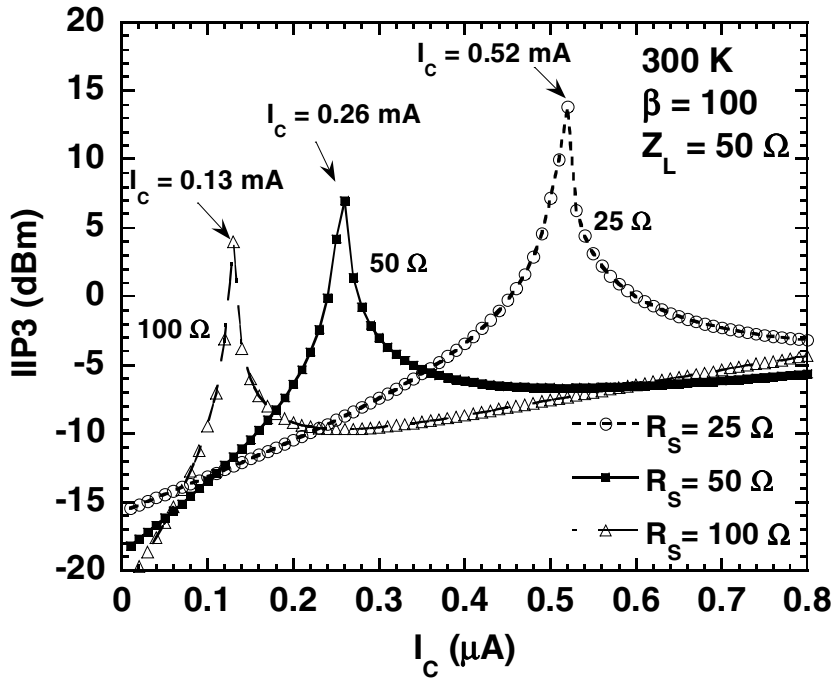

Figure 94: Low-current CB IIP3 calculated using Volterra series for R_S = 25, 50, and 100 Ω. I_C where the low-current ($I_{NL3-g_m} = 0$) IIP3 peak occurs is indicated.

peak to be

$$I_{C(I_{NL3-g_m}=0)} = \frac{kT/q}{R_s(2 - 1/\beta)}. \tag{62}$$

This expression shows that the current at this IIP3 peak is proportional to $1/R_S$, and that β has a small influence for realistically large values. For example, at room temperature (kT/q = 26 mV), if R_S is increased from 50 to 100 Ω, this peak will shift from I_C = 260 to 130 μA. This observation is confirmed by Volterra series computations (shown in Figure 94) and harmonic balance simulations, both of which show excellent agreement with Equation 62 for different R_S values.

5.4.4 Comparison with Simulated Results

Predicting linearity response for different Z_L is important for the design of linear CB and cascode amplifiers. Figure 85 showed already that the design kit model was well matched to measured data with respect to high-current linearity degradation. The accuracy of Volterra series calculations should likewise be evaluated, with particular emphasis on its capability of properly capturing trends across bias and Z_L.

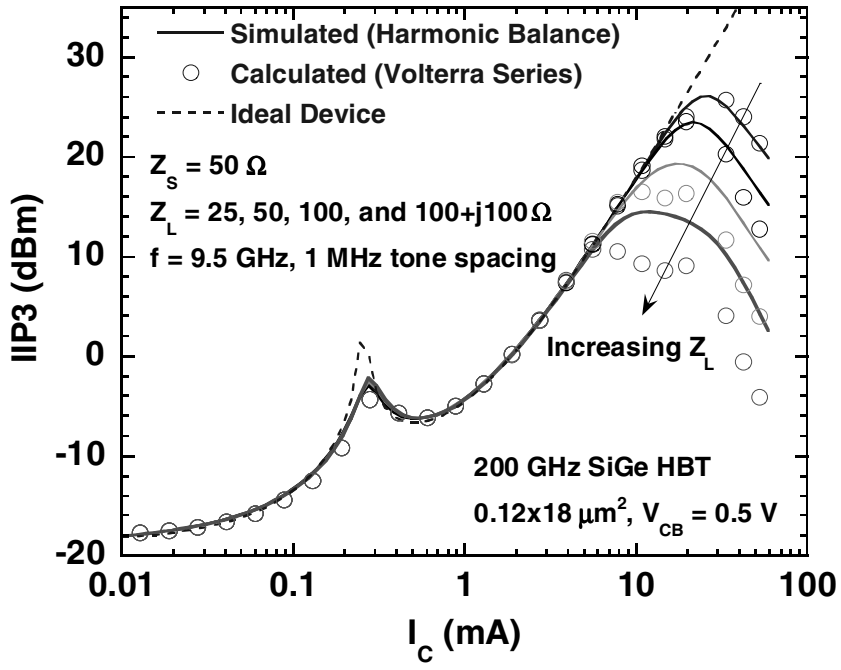

Figure 95: Comparison between VBIC model simulation (solid lines) and Volterra series (open circles) of CB IIP3 for a 200 GHz SiGe HBT ($A_E = 0.12\text{x}18\mu\text{m}^2$) at different Z_L.

The nonlinearity coefficients for a 200 GHz SiGe HBT ($A_E = 0.12\text{x}18\mu\text{m}^2$) were extracted and results of the CB Volterra series computations were compared with harmonic balance simulations using the design kit model for the same 200 GHz SiGe HBT. A variety of load impedances were examined. Figure 95 shows that the calculated IIP3 across bias using Volterra series closely matches the model simulation, even as Z_L is increased from 25 Ω to 100 + j100 Ω. The IIP3 for the "Ideal Device," which is geometry independent and does not suffer from high-injection effects, is shown for comparison. Both the computed and simulated results show that linearity begins degrade at lower I_C (and consequently, peak IIP3 is reduced) as $|Z_L|$ increases. For larger Z_L a discrepancy is observed at high-current between the calculated and simulated results. Even so, linearity trends across Z_L are reliably predicted by the CB Volterra series analysis, as shown in Figure 96, which plots peak IIP3 (calculated and simulated) as a function of the real (R_L) and imaginary (X_L) parts of Z_L.

The current (I_C) at which linearity begins to degrade is perhaps of even greater concern, and this value is compared (calculated and simulated) across Z_L in Figure 97, which plots the I_C where

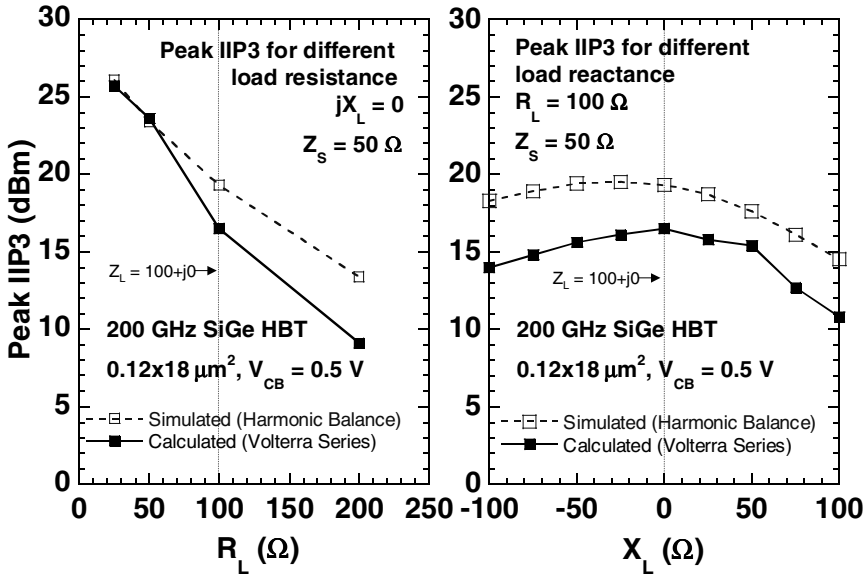

Figure 96: Comparison of simulated and calculated peak CB IIP3 for the 200 GHz SiGe HBT as a function of Z_L $(= R_L + jX_L)$: (left) R_L for $jX_L = 0$, and (right) X_L for $R_L = 100$.

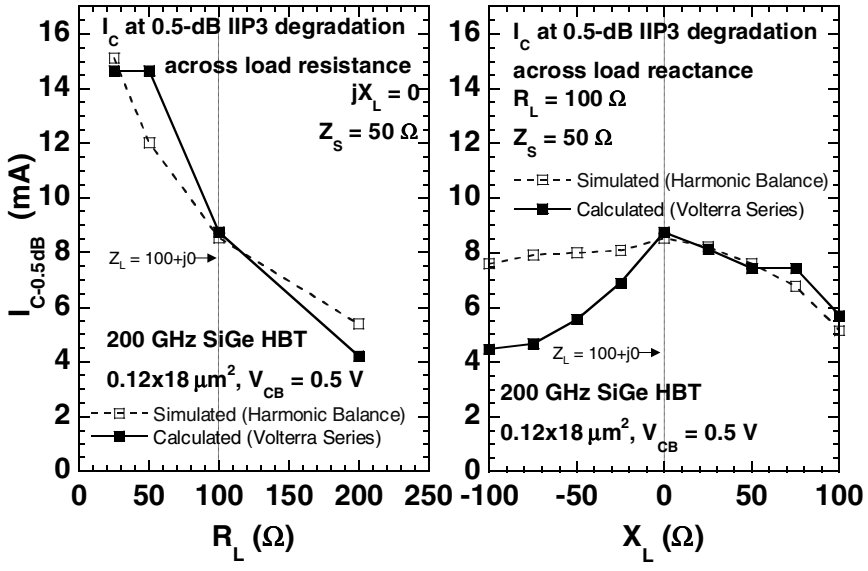

Figure 97: Comparison of simulated and calculated CB 0.5 dB IIP3 degradation current ($I_{C-0.5dB}$) for the 200 GHz SiGe HBT as a function of (left) R_L for $jX_L = 0$, and (right) X_L for $R_L = 100$.

IIP3 has degraded by 0.5 dB with respect to IIP3 of the "Ideal Device" ($I_{C-0.5dB}$). This degradation point is well-matched between calculation and simulation across R_L and for $X_L > 0$. For $X_L < 0$, Volterra series tends to underestimate $I_{C-0.5dB}$ compared to the simulation. Overall, the Volterra series analysis presented here shows excellent agreement with measured and simulated data, and its ability to capture and predict key linearity trends across device bias and load impedance has been confirmed. The high-current linearity degradation observed for high load impedances can be accurately described by the third-order C_{bc} nonlinearity, and the low-current linearity peak is described as a self-cancellation in the g_m nonlinearity that occurs near $I_C = V_T/2R_S$. Overall, simpler expressions for intermodulation distortion provide greater insight into the fundamental impact of device and circuit parameters on linearity performance.

CHAPTER VI

DESIGN OF SIGE HBT CIRCUITS FOR ENHANCED DYNAMIC RANGE

6.1 Introduction

By applying the new understanding of the device-level operating limits and linearity performance of SiGe HBTs, two high-frequency transceiver circuit blocks demonstrating enhanced dynamic range performance were designed, fabricated, and tested. Both circuits were designed at X-band for radar applications. The first design is a high-gain two-stage low noise amplifier (LNA), which uses a novel combination of large-signal and small-signal design strategies to achieve an aggressive set of specifications targeting high-dynamic range performance. The second design is single-stage cascode power amplifier (PA), which uses an aggressive collector bias to achieve higher output power without increasing the active transistor area.

6.2 High Dynamic Range (HDR) SiGe X-Band LNA

6.2.1 Motivation

Although the dynamic range of a receiver system can be limited by a variety of components, the low-noise amplifier (LNA) presents important challenges because of the requirements for (a) low noise, (b) high gain and (c) low power consumption. As the first gain stage in a receiver chain, the LNA has a strong impact on the dynamic range performance, directly impacting both the system noise figure and the system linearity.

For example, consider the SFDR performance of an RF front-end-module (FOM) consisting of a typical high-performance LNA (20 dB gain, 1.5 dB noise figure, and input third-order intercept point of 0 dBm) cascaded with a receiver block with gain of 10 dB and 1 MHz bandwidth. To achieve a SFDR of 70 dB, the noise figure of the receiver block would have to remain below 10 dB. However, if the 20-dBm LNA was replaced by an high-dynamic range (HDR) LNA with and identical noise and input-linearity (IIP3) but 30 dB gain, the noise requirements of the following receiver block can be significantly relaxed, allowing its noise figure to increase to 15 dB while maintaining the same overall SFDR [27]. By the same token, the overall SFDR can be improved by

as much as 3 dB for a given receiver noise figure using the proposed HDR LNA.

This analysis clearly shows the benefits of a high-gain, high-linearity LNA for improving receiver dynamic range performance. Currently, LNAs that achieve this level of performance typically use HEMT technologies and require the circuit to be fabricated in costly III-V processes. Therefore, achieving comparable performance using a low-cost Si-based solution (such as SiGe BiCMOS) is desirable [27].

6.2.2 LNA Design

The LNA presented here was designed to achieve OIP3 of 30 dBm, over 30 dB of gain, and less than 2 dB noise figure (NF) for operation at X-band frequencies (8.5 to 10.5 GHz). In addition, a ± 0.5 dB gain-flatness across 2-GHz and *dc* power dissipation of less than 300 mW was specified. The input and output impedances should be well-matched to 50 Ω to maintain a low voltage standing wave ratio (VSWR). A 0.13μm third-generation SiGe BiCMOS platform (IBM 8HP) with an f_T /f_{max} of 200/280 GHz was chosen for this design [57].

Even with the high-performance HBT offered in this SiGe process, achieving 30 dB of gain at X-band requires multiple gain stages. Therefore, a two-stage approach was chosen for this LNA design. However, using a second-stage introduces significant challenges in terms of linearity compared to a single-stage design. From the cascaded linearity calculation in Equation 5, it is clear that the *input*-IP3 of the second-stage must be some margin higher than the *output*-IP3 of the first-stage in order to not degrade to overall linearity of the LNA. At the same time, high gain (and therefore high OIP3) is required at the first-stage to minimize the overall NF of the circuit.

Because of these demanding requirements, a novel combination of both small-signal and large-signal amplifier design methodologies were used to design the high-dynamic range (HDR) LNA. A schematic of the two-stage LNA is presented in Figure 98. The performance goals for each stage, along with the overall performance goals for the HDR LNA, are summarized in Table 7.

An inductively-degenerated cascoded LNA, which is discussed in [71], was used for the first-stage. The design priorities for this stage were focused on standard (small-signal) LNA performance metrics: achieving high gain and low NF. This required transistor sizing and bias for optimal gain and noise while achieving the desired linearity performance. Increasing the collector current to

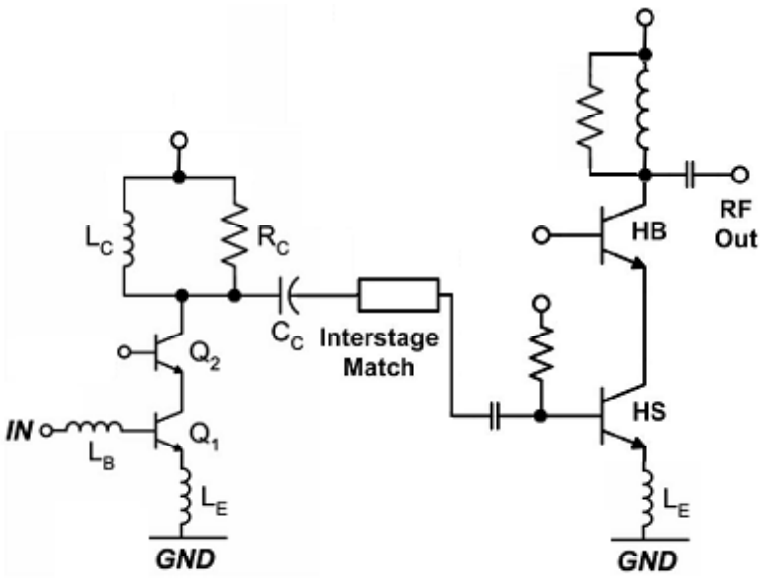

Figure 98: Schematic for two-stage HDR LNA with noise matched first-stage and power-matched second-stage.

Table 7: Design targets for the two-stage X-band HDR LNA: input stage, output stage, overall.

	Stage 1	Stage 2	Overall
Gain (dB)	20	10	30
IIP3 (dBm)	0	> 20	0
NF (dB)	1.5	–	< 2
S_{11} (dB)	< -10	–	< -10
S_{22} (dB)	–	<-10	< -10
P_{dc} (mW)	40	< 260	< 300

achieve better linearity will tend to degrade the noise performance, so an optimal balance between the two metrics was required in order to achieve IIP3 of 0 dBm without excessive sacrifice to NF. A high gain of 20 dB was targeted for this stage to ensure that the overall NF for the HDR LNA is dominated by the carefully-tuned noise performance of the first-stage.

This research is primarily focused on the design of the second-stage and integration of the full two-stage LNA. To achieve the overall OIP3 specification of 30 dBm, it follows from a general rule-of-thumb that the output P1dB of the second-stage should be around 20 dBm, which is similar to the power-handling capability of X-band SiGe PAs reported in the literature [6]. Therefore, the design of second-stage of the HDR LNA was primarily focused on providing adequate large-signal performance to achieve the required linearity for the overall circuit. The transistor core of the second-stage is comprised of a high-performance/high-breakdown (HS/HB) cascode structure, which includes eight parallel HS common-emitter HBTs (each sized at 0.12 x 18 μm^2) driving eight parallel HB cascoded HBTs (each sized at 0.6 x 18 μm^2). The one-to-five ratio in device area was required to match the peak-f_T current between the HS and HB devices, so a custom layout and model was generated in order to utilize the 0.6 μm-wide device. This transistor core is capable of providing over 20 dBm of output power under large-signal operating conditions [6]. However, for this design the high-*current* handling capability of the parallel HBTs is used to provide the necessary linearity under small-signal operating conditions.

Figure 99 shows the simulated linearity performance of the second-stage cascode core for different collector voltages as a function of quiescent current bias (I_C) and *dc* dissipated power. As expected, biasing at higher collector current or voltage can significantly improve OIP3, and based on these results the design point of 48 mA at 5 V (240 mW) was selected. To achieve an IIP3 of over 20 dBm (assuming OIP3 of over 30 dBm), the gain of the second-stage was reduced using inductive degeneration at the emitter, with simulation results shown in Figure 100. This reduction is acceptable since only 10 dB of gain is required at the second-stage. In addition to increasing IIP3, however, OIP3 is increased as well, owing to the linearizing effect of this local feedback [14]. An inductor value (L_E) around 8 nH shows the optimal linearity performance. Ultimately, however, a more conservative design value of 12.5 nH was selected in order for best balance gain, stability, bandwidth, and linearity of the stage.

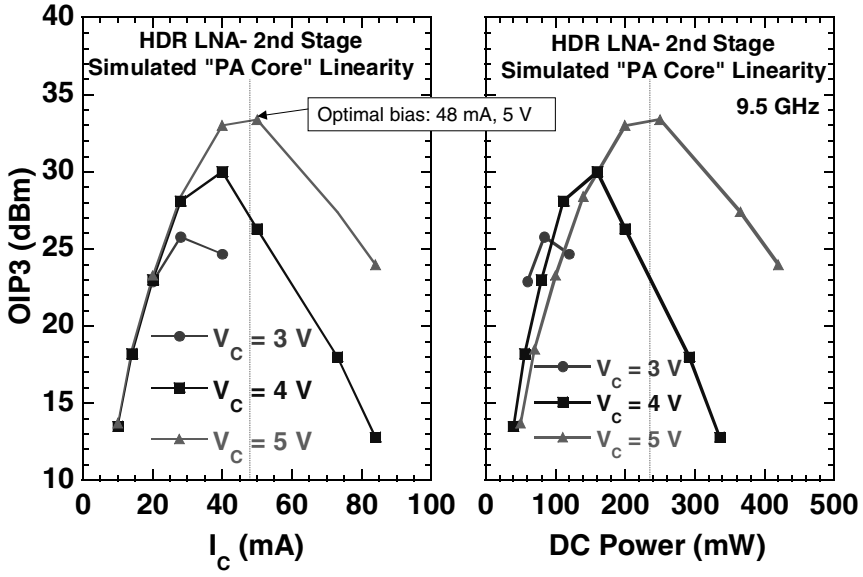

Figure 99: Simulated linearity of the output-stage cascode transistor core as a function of (left) collector current, and (right) dissipated *dc* power.

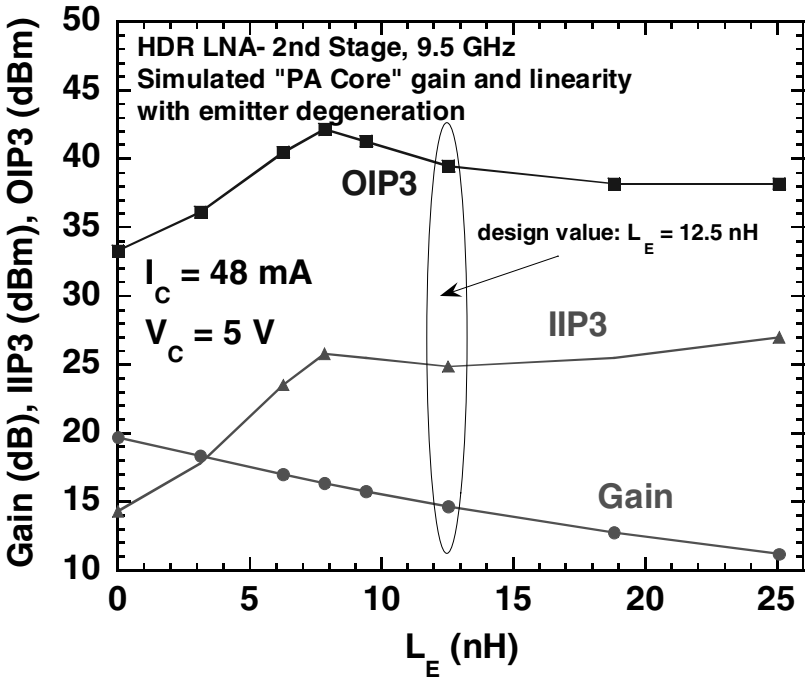

Figure 100: Simulated gain and linearity of the output-stage cascode transistor core as a function of emitter degeneration inductance.

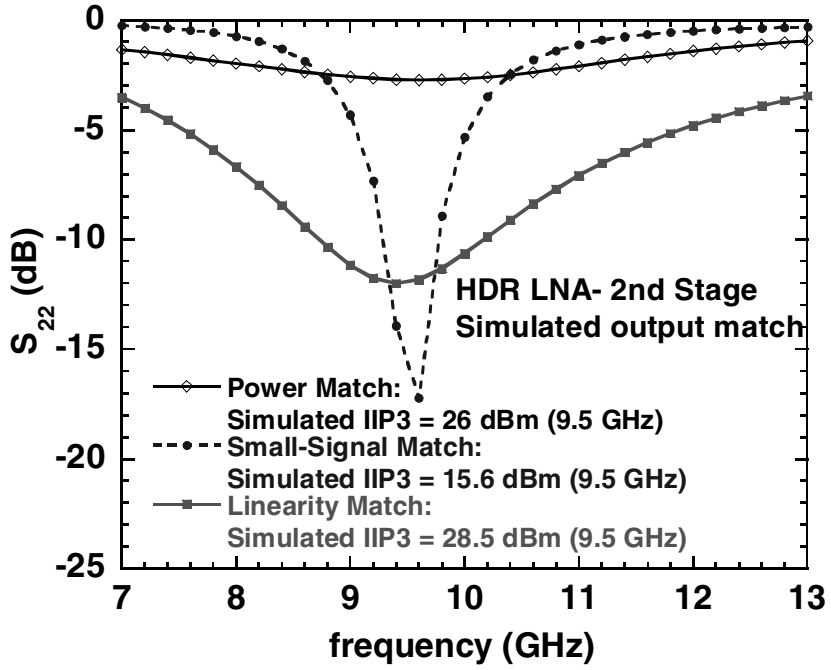

Figure 101: Simulated S_{22} for the output stage for different output matching networks.

As discussed in Chapter V, the load impedance can significantly affect the linearity performance of the common-base (output) transistors in the cascode core. This effect was observed during the design of the HDR LNA output stage, and played an important role in the design of the output match for the stage. Sufficient linearity performance (IIP3 = 26 dBm with 11 dB gain) was achieved when the output was large-signal matched. However, this output match resulted in poor output reflection (S_{22} above -3 dBm) as shown in Figure 101, which results in mismatch and high VSWR for small-signal operation. When the output of second-stage was small-signal (conjugate) matched, the output reflection was significantly improved, but the linearity degraded significantly with over 10 dB reduction in both IIP3 and OIP3. An optimal compromise between output reflection and linearity (the "Linearity Match") was accomplished by placing a resistor (181 Ω) in parallel with the shunt (RF choke) inductor in the output matching network. This matching network design shows much better output reflection than the large-signal match, and superior linearity to the small-signal match, maintaining IIP3 above 28 dBm with 11 dB gain.

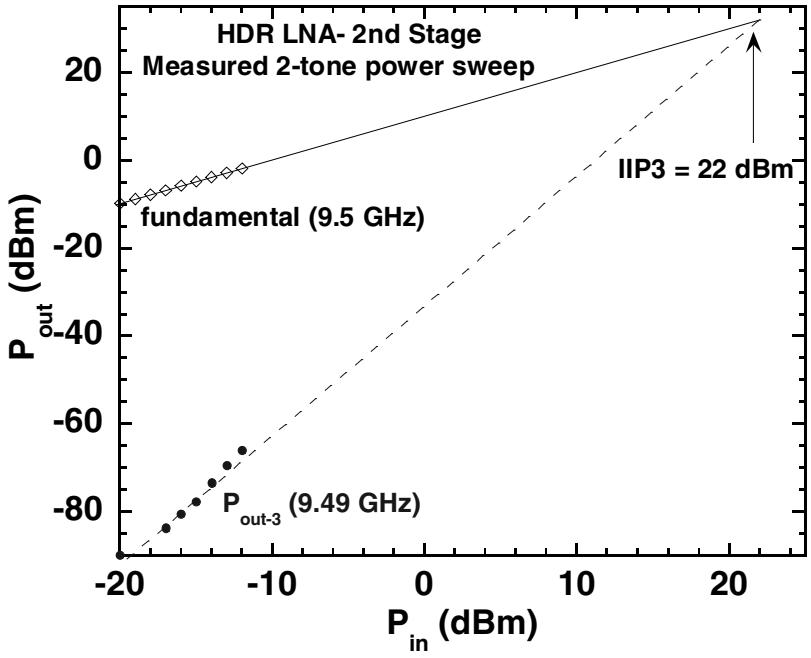

Figure 102: Measured fundamental (9.5 GHz) and third-order intermodulation (9.49 GHz) output tones with intercept point extrapolation for the output stage of the HDR LNA.

6.2.3 Measured Results

6.2.3.1 Output Stage Results

To first verify the performance of the output stage of the two-stage HDR LNA, it was fabricated and measured independently as a separate subcircuit block. The measured s-parameters of the output stage subcircuit show the desired gain with S_{21} of just over 10 dB, good isolation (S_{12} < -48 dB), and adequate input and output reflection. The measured two-tone results for the output stage subcircuit in Figure 102 show that IIP3 was around 22 dBm, several dB lower than expected from simulation. This result is still above the required value of 20 dBm for the stage, although has less additional linearity margin than desired. The measurement-to-simulation discrepancy in linearity is attributed to limitations in the higher-order accuracy of the custom wide-emitter HB model used during simulation. Intended for large-signal (PA) applications, this model was calibrated to *dc*, *ac*, and large-signal behavior, but did not explicitly consider linearity.

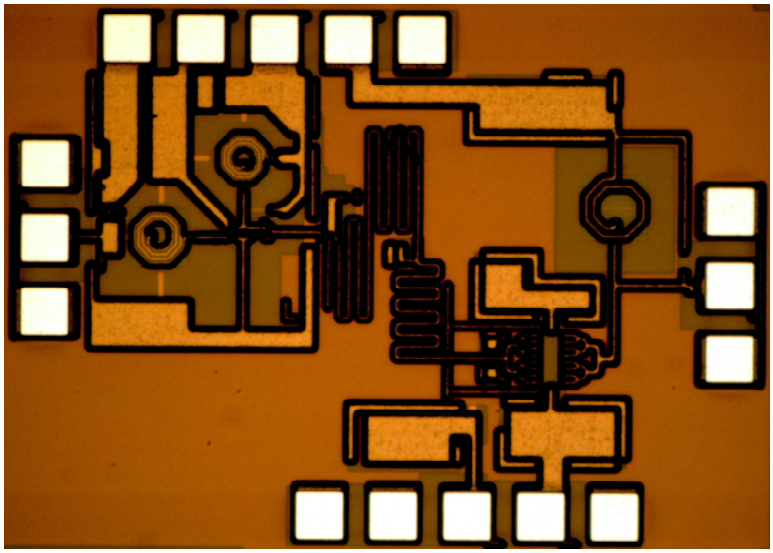

Figure 103: Micro-graph of fabricated two-stage HDR LNA.

6.2.3.2 LNA Results

The a die-photo for the measured two-stage HDR LNA is shown in Figure 103. This circuit was fabricated in a 0.13 μm BiCMOS technology with seven metal layers and fully suite of mmW-passive components. The total area is 1.6 x 1.1 mm^2 including on-chip matching networks and bondpads. The measured s-parameters for the HDR LNA are shown in Figure 104. The LNA shows an (S_{21}) greater than 30 dB with 2.5 GHz of bandwidth with gain flatness of better than ± 0.5 dB. The input return loss is below -15 dB across the band, which is required to prevent a high-VSWR towards the antenna element.

The linearity of the HDR LNA was measured with a fundamental tone at 9.5 GHz with a second tone offset by 10 MHz. Figure 105 plots the fundamental output power at 9.5 GHz and the lower order IMD product at 9.49 GHz, with extrapolation showing the OIP3 to be over 29 dBm with a gain of 30 dB. The 50 Ω noise measurement results in Figure 106 show a 2 dB NF between 8.5 and 10.5 GHz and 1-dB noise impedance circles at 9.5 GHz are shown in the figure inset. This measurement across source impedance shows the center of the noise circles located near 50 Ω, indicating that the LNA is well noise matched. In addition, NF remains below 3 dB even for input mismatches up to a VSWR of 3:1.

This work represents the first reported Si-based X-band LNA to achieve OIP3 of roughly 30

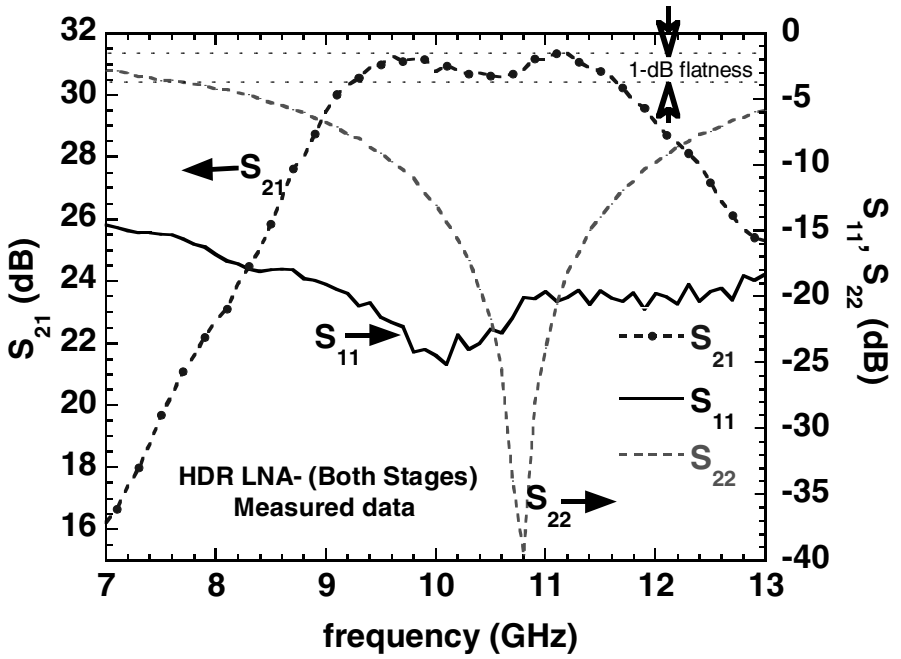

Figure 104: Measured gain (S_{21}) and return loss (S_{11} and S_{22}) for the full two-stage HDR LNA.

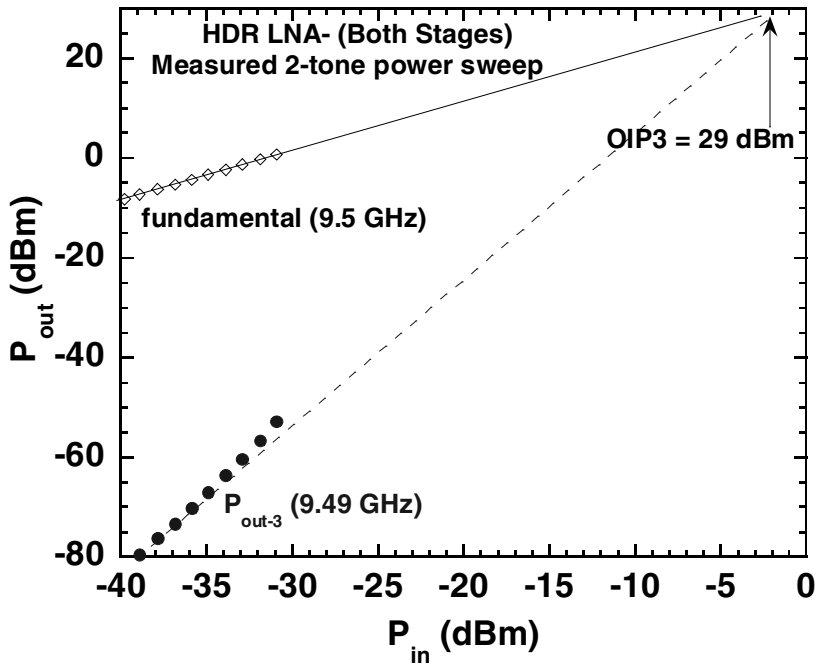

Figure 105: Measured fundamental (9.5 GHz) and third-order intermodulation (9.49 GHz) output tones with intercept point extrapolation for the full two-stage HDR LNA.

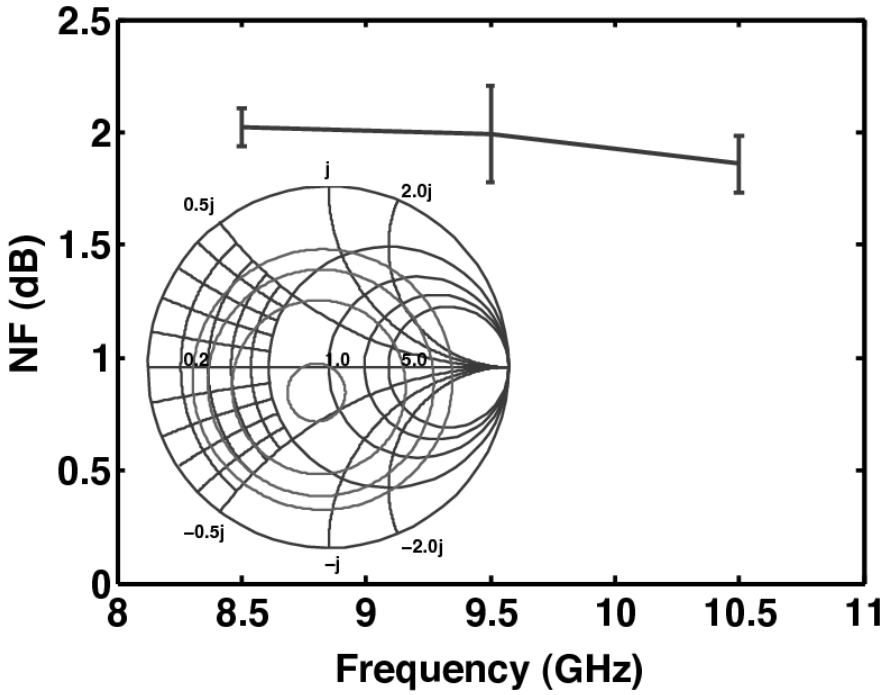

Figure 106: Measured 50 Ω noise figure at 8.5, 9.5, and 10.5 GHz with error bars highlighting measurement uncertainty, and inset depicting calculated noise circles on source impedance at 9.5 GHz.

dBm with a noise figure of 2 dB. The performance of this circuit is benchmarked with other high-linearity LNAs from the literature in Table 8 using the figure-of-merit presented in [27]. The performance of this circuit is competitive with or superior to state-of-the-art HEMT-based LNAs fabricated in more costly III-V technologies. Overall, the design of this HDR LNA highlights the capabilities of SiGe HBT technology to improve receiver performance by simultaneously providing both low noise and high-linearity performance suitable for a wide range of receiver applications.

Table 8: Comparison with other High-Linearity LNAs

Ref.	Freq. (GHz)	NF (dB)	Gain (dB)	P_{diss} (mW)	OIP3 (dBm)	OP1dB (dB)	Technology	FOM (dBm)
This Work	9.5	2	30	285	29	18.5	200 GHz SiGe HBT	39.5
[71]	10	1.36	19.5	15	20.3	10	200 GHz SiGe HBT	37.5
[72]	6	2.7	10.8	540	22.8	12.8	AlGaN/GaN HEMT	21.1
[73]	6	1.6	10.9	120	23	13	GaN HEMT	29.1
[74]	8.5	0.53	32	109	20.5	10.5	GaAs mHEMT	28.7

6.3 Aggressive-Cascode X-Band 24 dBm PA

6.3.1 Motivation

As discussed in the introductory chapter of this thesis, obtaining high output power from SiGe HBTs for power amplifier (PA) applications remains an important challenge due to their relatively low breakdown voltages, and this goal becomes increasingly difficult at higher operating frequencies. Demonstrated in Chapter V, the cascode configuration can increase the output voltage swing of the SiGe HBT for higher power handling capability. A "mixed-cascode" approach, which uses a low-breakdown (HS) common-emitter transistor cascoded with a high-breakdown (HB) common-base transistor, has been reported previously [6], and this technique has been utilized to obtain near 1-Watt SiGe PA performance at X-band frequency [56].

Because of reliability concerns at high collector voltage, these designs tend to avoid biasing at V_C beyond the base-current reversal point for the output transistor, which is consistent with standard practice. Therefore, higher output power is typically achieved using higher operating currents, requiring that the active device area is increased by placing additional transistors in parallel. The reported X-band 1-Watt SiGe PA, for example, uses a large bank of 128 parallel cascode HBT cores [56]. However, increasing the active device area has several drawbacks.

1. The output impedance of the PA is reduced as device area increases, making impedance transformation to 50 Ω more difficult. For a given quality factor (Q) of the passives at higher frequencies, a single-stage transformation to lower impedance will suffer from reduced bandwidth. A more complex multistage matching network can be utilized to maintain bandwidth, but will suffer from additional losses in the passives, which degrades output power and PAE.

2. Additional levels of power-combining are required as the size of the transistor bank increases, which results in additional losses. Off-chip (board-level) power combining and matching can reduce these losses, but is more complex and requires a larger footprint than a fully-integrated solution.

3. The collector-to-substrate capacitance increases with active device area, and may incur additional performance losses.

4. Electro-thermal interactions between adjacent cores become more problematic as more devices are operated in parallel, and can cause *dc* and high-frequency instabilities.

As these losses add up and degrade the amplifier efficiency, more *dc* power is required to reach the targeted RF power, which exacerbates the thermal issues in PA. The net result is a condition of diminishing returns as the number of parallel transistors grow larger. Using the aggressive bias approach discussed in Chapter 4, the cascode PA presented here aims to sidestep these drawbacks. By increasing the output voltage swing of the SiGe PA, the aggressive cascode design can reduce the total transistor area required to achieve a given output power, while increasing efficiency and maintaining reliable operation.

6.3.2 PA Design

The circuit presented here was based on a previously published 100 mW (20 dBm) X-band SiGe PA operating from a 5 V supply [6]. The design modified to achieve 250 mW (24 dBm) output power and over 20 dB gain from a single stage, while maintaining the same active transistor area with a mixed-cascode transistor core identical to the one used in the original design. A schematic of the single-stage PA is presented in Figure 107.

The PA core is comprised of eight parallel HS/HB cascodes (each sized at 0.12 x 18 μm^2 and 0.6 x 18 μm^2, respectively) and includes a resistive base feed (50 Ω per device), which serves as a portion of the input match while providing *dc* base voltage to the input device and increasing small-signal stability. The output match consists of a shunt *dc*-feed inductor and series *dc*-blocking capacitance. Both the input and output are matched to a nominal system impedance of 50 Ω. All *dc*-bias lines are connected to RF bypass capacitors near the active transistor core, in order to shunt RF energy on these *dc* nodes to ground and ensure *ac* stability. This circuit was designed and fabricated using a 0.13 μm third-generation SiGe BiCMOS platform (IBM 8HP) with an f_T /f_{max} of 200/280 GHz [57].

The PA was biased for Class AB operation, with the input base voltage V_{BB} = 0.9 V and the cascode base voltage V_{CA} = 2 V to maximize output voltage swing. The collector voltage (V_{CC}) was raised beyond 5 V to increase the output power, as shown in the simulated results in Figure 108. This result shows that simulated output P1dB rises from 18.5 dBm to 24.4 dBm and the saturated

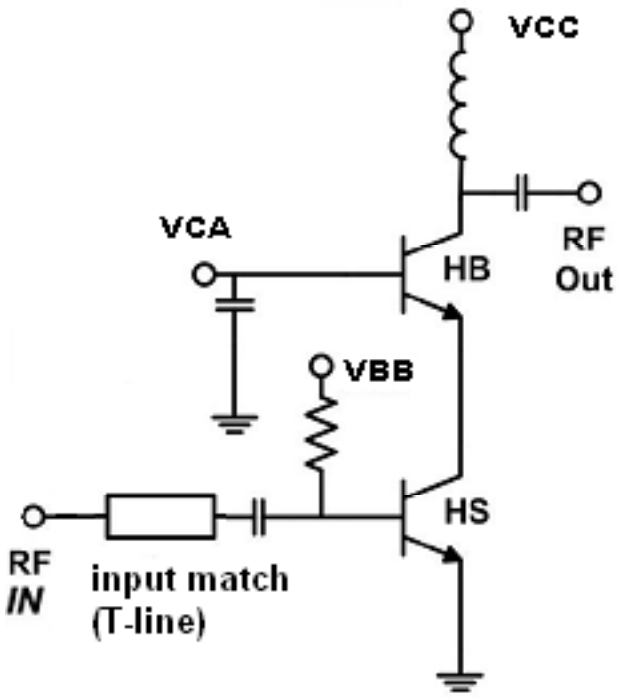

Figure 107: Schematic for the single-stage X-band cascode PA.

output power increases by 3 dB as V_C is increased from the standard operating point at 5 V to an aggressive operating point at 7.5 V. Moreover, this performance enhancement is accompanied by an improvement to PAE.

However, there are practical upper-limits to the collector voltage bias, such as the dynamic SOA and pinch-in effects discussed in Chapter 4. In particular, since the pinch-in effect is not captured by standard device models, this limit should be determined and kept in mind during design. Figure 109 shows a *dc* bias sweep of the collector voltage of the cascode core at the Class AB operating point. The pinch-in limit is indicated by the discontinuity in the output current characteristic around 6.7 V. From this result, the aggressive cascode design point of $V_C = 6$ V is selected to maintain a reasonable margin below the pinch-in threshold. Next, load- and source-pulls were performed in simulation at this design point to determine the optimal source and load impedances for maximum output power. Impedance transformation networks were designed to match these impedances back to 50 Ω at the source and load.

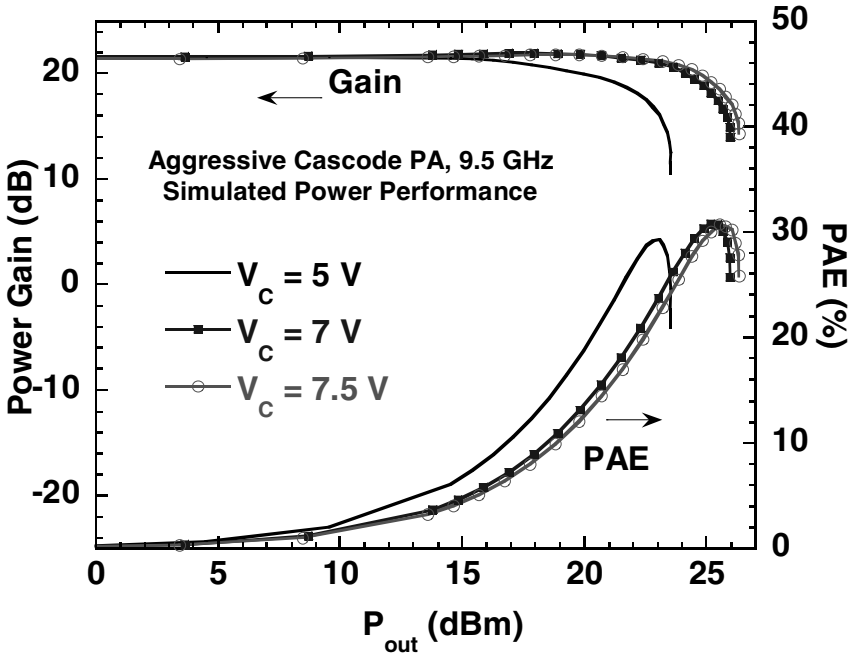

Figure 108: Simulated power gain and PAE as a function of output power for the cascode PA for "standard" (5 V) and "aggressive" operation at higher collector voltage.

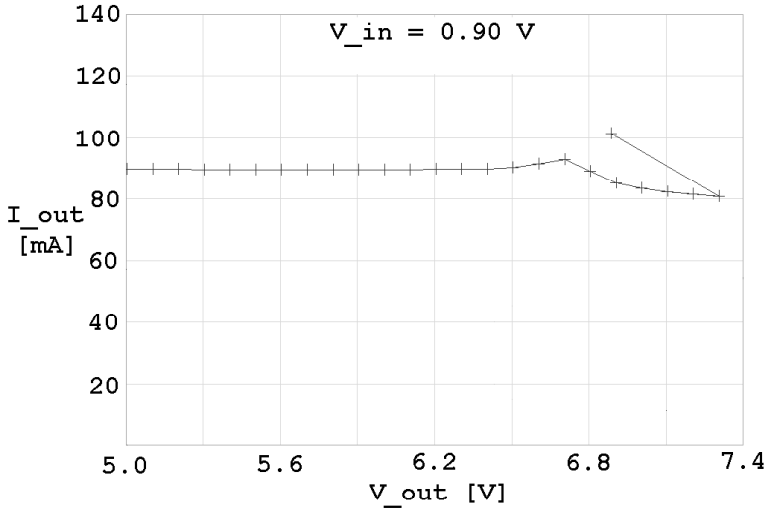

Figure 109: Measured *dc* output characteristic of the cascode PA core showing the pinch-in instability point (near $V_C = 6.7$ V) for $V_{BE} = 0.90$ V.

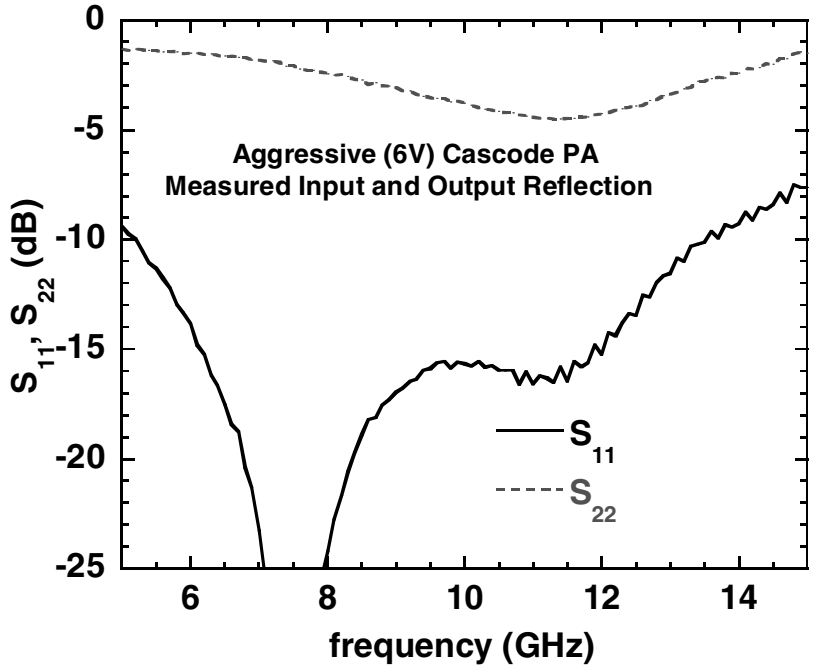

Figure 110: Measured input (S_{11}) and output (S_{22}) return loss across frequency for the aggressive cascode PA.

6.3.3 Measured Results

Figure 110 shows the small-signal input and output match measured across frequency for the aggressive cascode SiGe PA. The S_{11} shows that the input is well-matched to 50 Ω across the band, while the large-signal output match shows a high S_{22} under small-signal operating conditions. To verify the load match under large-signal conditions, a load-pull was performed on the PA for high input-power at 9.5 GHz. The result of this measurement in Figure 111 shows that the saturated output power contours peak near 24 dBm at $Z_L = 50\ \Omega$, confirming that the PA is well-matched at the load.

The measured power sweep at 9.5 GHz in Figure 112 shows that by moving to a 6 V bias, the aggressive cascode PA design is capable producing output power up to 24 dBm, considerably higher than the standard (5 V) design. Power gain and PAE as a function of output power at 9.5 GHz are compared for the two designs in Figure 113. The aggressive cascode PA has a measured output P1dB of 22.8 dBm, which is a 2.1 dB improvement over the standard design. In addition, the gain is increase by over 1 dB and peak PAE improves from less than 26% to almost 30%.

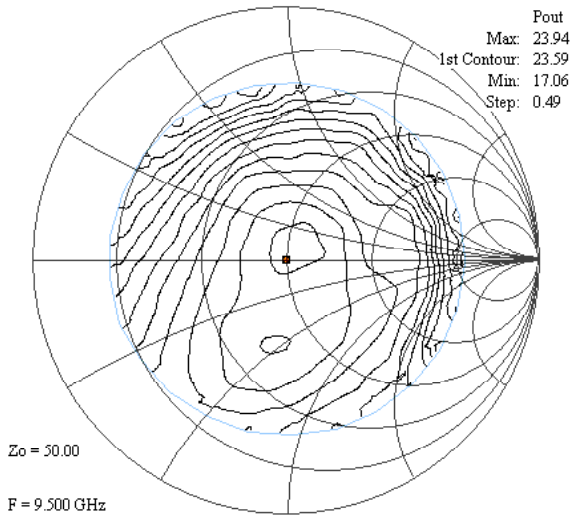

Figure 111: Measured output power contours (0.5-dB per step) for a load-pull performed on the aggressive cascode PA at 9.5 GHz with P_{in} = 5 dBm.

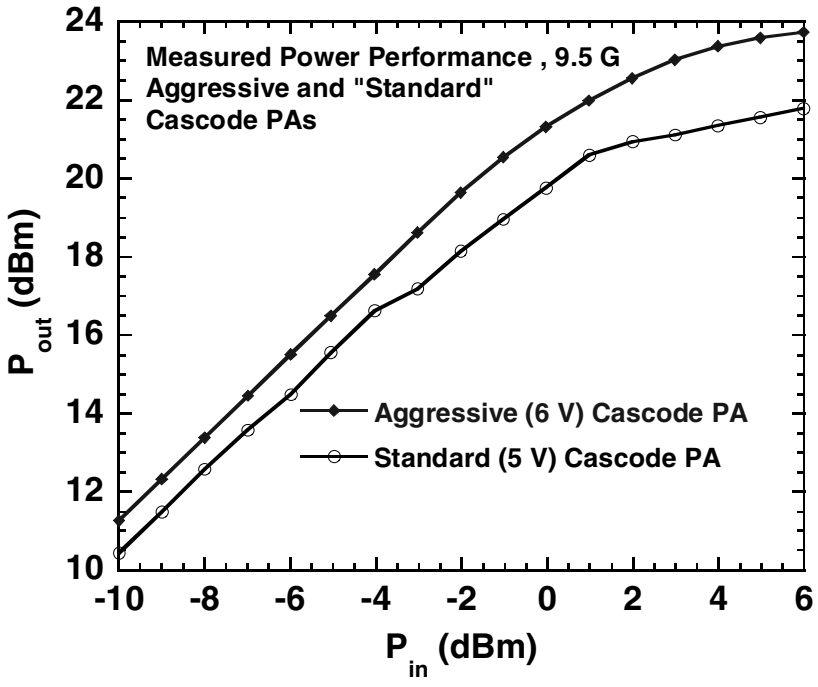

Figure 112: Measured power sweep for the aggressive (6 V) cascode PA compared to the standard (5 V) cascode PA at 9.5 GHz.

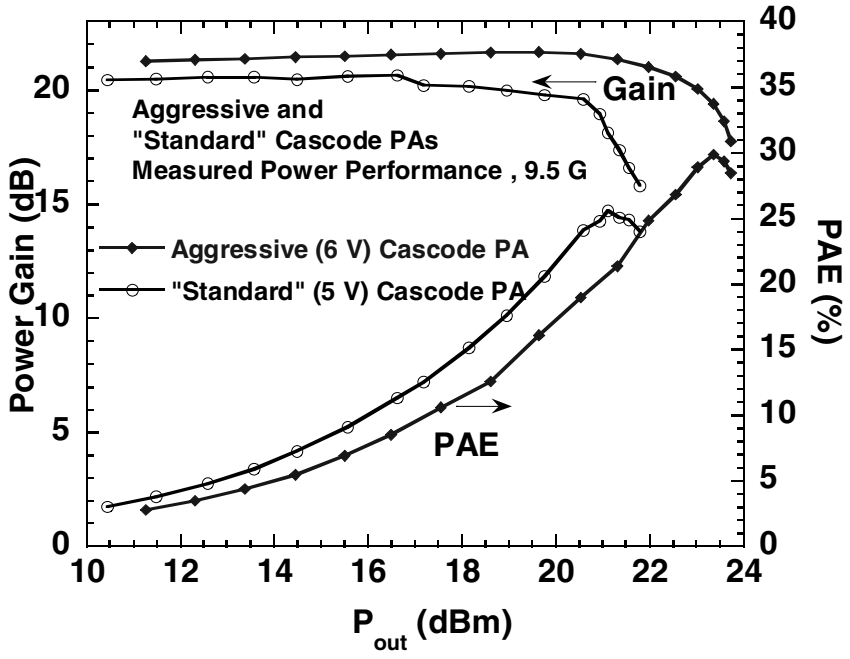

Figure 113: Measured power gain and PAE as a function of output power for the aggressive (6 V) cascode PA compared to the standard (5 V) cascode PA at 9.5 GHz.

The RF safe-operating area (SOA) limits, discussed in Chapter 4, were examined for the aggressive cascode PA to ensure reliable operation at high RF power. These results are plotted in Figure 114, which shows the operating point of the PA (x) with respect to the voltage-limited RF failure threshold ($P_{out-fail-V}$) calculated across V_C using Equations 41 and 43. For comparison, the RF SOA limit for the low-breakdown cascode (at Z_L = 43 + j64 Ω, identical to the example presented in Chapter 4) is also plotted. For the high-breakdown output device (BV_{CBO} = 12 V) driving the optimal load impedance for the PA (Z_L = 16 + j24 Ω), this limit was determined to be around 26.3 dBm at V_C = 6 V. This limit is a safe margin above the 24 dBm saturated output power for the PA, confirming that its dynamic voltage limit will not be exceeded during large-signal operation.

To avoid exceeding the current-limited dynamic SOA limit, attention was paid during the design of this circuit to ensure that the V_C operating point (at 6 V) was below the pinch-in threshold, as shown in Figure 109. Additional power measurements were performed at higher collector bias voltages up to 7 V, exceeding the pinch-in limit. Under these excessive voltage bias conditions

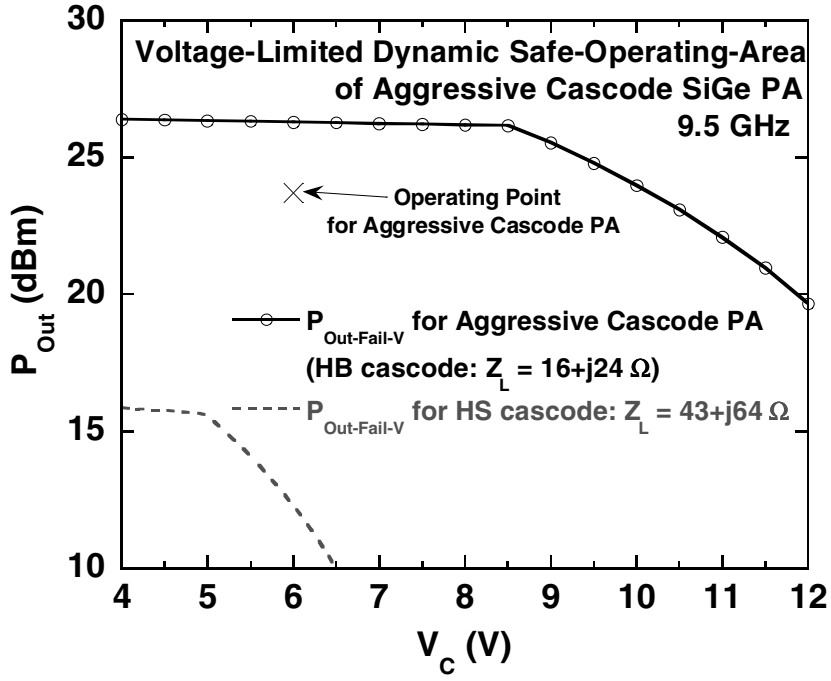

Figure 114: The RF SOA across V_C for the aggressive cascode PA, plotted with the operating point (x) for the PA. The RF SOA for the HS cascode examined in Chapter 4 is plotted for comparison.

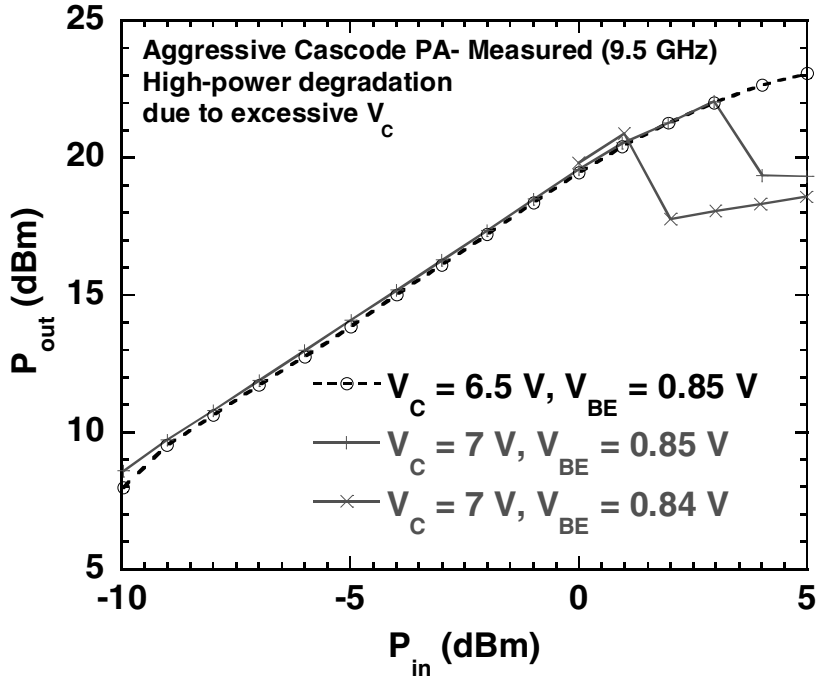

Figure 115: Measured power sweep for the aggressive cascode PA showing RF power degradation for excessive (7 V) collector bias.

the PA consistently experiences a sudden degradation in output power as input power is increased. Figure 115 shows this degradation at high P_{in}. This result indicates that, in addition to degrading the reliability of a PA, pinch-in effects can also severely degrade the RF performance under large-signal operating conditions. It should be noted also that this degradation is not captured in simulation, since the standard compact models do not account for pinch-in effects. However, at its proper operating point, the aggressive cascode PA design presented here successfully increases the output power for a given device area while maintaining a reasonable margin within the RF safe-operating area and below the threshold for pinch-in instabilities.

CHAPTER VII

CONCLUSION

7.1 Contributions

Operating voltage constraints and linearity pose critical limitations to dynamic range for emerging high-frequency transceivers, so a primary focus of this thesis has been to achieve a comprehensive understanding of the transistor-level limits and performance trade-offs of state-of-the-art SiGe HBTs for these future systems. Avalanche breakdown effects, reliability and safe-operating area, and intermodulation distortion were all examined in detail as part of this comprehensive study. The contributions of this work can be summarized as follows:

1. A comprehensive analysis of the effects of scaling and bias on operating voltage constraints in advanced SiGe HBTs has been presented. It was shown that trans-generational device scaling for increased peak f_T performance in SiGe HBTs is accompanied by compression of their operational voltage limits, and that for all three SiGe HBT generations the common-base with forced I_E bias configuration allows a substantially higher maximum collector voltage than does the common-emitter with forced I_B configuration.

2. A novel approach was introduced to analyze the factors contributing to common-base avalanche instabilities in SiGe HBTs. This work highlighted for the first time the distinct regions of instability behavior across bias and introduced new parameters that describe the bias dependence of pinch-in effects and provide physical insight into these often complex pinch-in characteristics observed in advanced SiGe HBTs. Comparisons were made across commercially available and next-generation SiGe HBT technology nodes using this novel approach.

3. Operating voltage constraints were investigated for SiGe HBTs operating in extreme environments for space-borne electronics applications. Both radiation and cryogenic operation were shown to cause a degradation to the pinch-in voltage, introducing potential reliability concerns for operation in the these environments. The novel pinch-in analysis was used to

obtain further insight at the device-level.

4. Large-signal RF performance, linearity, and reliability of cascode SiGe HBTs were investigated under aggressive collector voltage bias conditions to examine the various impacts that avalanche effects, such as base-current reversal and pinch-in, have on power amplifier operation. This work demonstrated that biasing in regions of strong base-current reversal does not degrade power performance, although avalanche multiplication nonlinearities contribute to higher intermodulation distortion and pinch-in effects can result in unpredictable fluctuations in RF gain.

5. A novel investigation of large-signal RF operating limits was presented for cascode SiGe HBT power amplifier cores, and new expressions were introduced to determine the large-signal safe-operating area under dynamic (RF) conditions. Catastrophic failures to the SiGe HBT were demonstrated when excessive RF power was applied at high collector voltage bias, or under conditions of pinch-in operation. Simple equations, which show excellent agreement with experimental data, were presented to predict the onset of device failure under both linear and compressed large-signal operating conditions.

6. Common-base intermodulation distortion for SiGe HBTs was investigated across bias, and new expressions that provide novel insight into linearity performance were derived from analysis using Volterra series. Linearity was characterized across collector current and collector voltage, and the roles of load match and collector design were examined. In particular, it was demonstrated that load matching for maximum gain can result in significant degradation in CB linearity at high current. Furthermore, it was demonstrated that both harmonic balance simulations and Volterra series calculations can closely predict common-base linearity characteristics.

7. The design and analysis of a high gain, high-linearity X-band low-noise amplifier for enhanced dynamic range performance was presented. The two-stage amplifier used a novel hybrid design methodology with the first-stage optimized for noise performance while the second-stage was optimized for linear high-power performance. This circuit represents the

first reported Si-based X-band low-noise amplifier to achieve nearly 30 dBm of output third-order intercept, 30 dB of gain, and a noise figure less than 2 dB. Moreover, this level of performance is competitive even with III-V based low-noise amplifiers.

8. The design and analysis of a 0.25-Watt X-band cascode power amplifier that achieves improved power density using aggressive collector voltage bias has been presented. By operating at higher collector voltage, it was demonstrated that higher output power and efficiency could be reliably achieved without increasing the active device area, with 2 dB improvement in the 1-dB compression point measured for this new power amplifier design. The operating point for the aggressive cascode power amplifier was confirmed to be a reasonable margin within the RF safe-operating area. Pinch-in effects were observed to degrade the RF performance of the circuit if excessive collector voltage bias was applied.

7.2 Future Work

Based on the research presented in this thesis, several excellent opportunities for future work should be considered. These areas of future study are summarized here.

The role that extreme environments play on breakdown and pinch-in effects for SiGe HBTs has been explored, but this research can be expanded further. For instance, the high-energy protons studied in this work will induce both ionizing and displacement damage to the semiconductor, and thus are regarded as worst-case in terms of radiation tolerance. However, studying pinch-in response for other particle types that induce only ionizing (i.e. gamma- or X-rays) or only displacement (i.e. neutrons) damage could bring further insight into radiation effects on operating voltage constraints. In addition, the study of voltage constraints and pinch-in effects for cryogenic operation provides groundwork for additional studies at high temperature. The reliability and performance of RF circuits in extreme environments is a topic also worth considering for further study.

The topic of linearity and dynamic range in SiGe HBTs is a broad area that warrants further study. The dynamic-range tensor, which currently examines device-level linearity trade-offs with gain, *dc* power, and operating limits for SiGe HBTs, would benefit by including noise figure in the analysis. This addition would provide a true examination of dynamic range in its full sense. Also, the distortion characteristics of common-emitter SiGe HBTs should be explored further using

Volterra series analysis in the same manner as the common-base analysis presented already. On-going work in this area has shown the common-emitter calculations to be much more sensitive to additional factors that do not significantly impact the common-base analysis. However, determining simple expressions for common-emitter linearity would prove extremely valuable for understanding the device-level linearity tuning knobs for SiGe HBTs and for developing a new figure-of-merit, which will provide greater insight and relevance in comparisons of linearity across technology.

In this work the RF stress and dynamic large-signal failure limits for SiGe HBTs were studied using high-frequency CW signals. In actual systems the amplitude of the RF input signal driving a power amplifier may be significantly varied or rapidly pulsed on and off. Further research in this area should examine high-frequency operating limits under pulsed-RF conditions to determine whether this realistic mode of operation will change the degradation patterns or failure characteristics of the SiGe HBT for better or worse.

The circuits presented in this work represent first-design passes, so further improvements and optimizations to these designs should be investigated. For the two-stage high-dynamic range low-noise amplifier, additional linearity and noise improvement to first-stage may be achieved by removing on-chip input *dc*-blocking capacitor. Also, measured results indicate that the custom high-breakdown SiGe HBT models used in the second-stage may be overestimating linearity performance in simulation. The studies presented on common-base linearity show that the low-breakdown device can achieve better linearity performance at high current than the high-breakdown device, so using the low-breakdown device may improve the linearity of the second-stage design.

The aggressive cascode power amplifier methodology presented in this work can provide the groundwork for future SiGe high-power amplifier designs. By placing two 0.25-Watt power amplifiers in parallel, in either a single-ended or differential configuration, the present design could be incorporated into an on-chip matched 0.5-Watt X-band power amplifier. At this power level, such a design could be suitable for the development of novel highly-integrated silicon-based phased-array radar systems. Maintaining independent operation of the two parallel power amplifiers is a key consideration in this future design and requires adequate thermal and electrical isolation between them. To ensure RF isolation and desired performance, the development of low-loss power combining networks, such as on-chip Wilkinson power combiners or baluns, is required.

APPENDIX A

MATLAB CODE

A.1 Dynamic Safe-Operating Area

Provided a collector bias point (VDC, IDC) and load impedance (RL, XL) this Matlab function uses Equations 41 through 46 to calculate and return the RF output power failure threshold in dBm (PMAX_dBm) for a specified dynamic voltage limit (VIMAX). Parameters capturing the knee-voltage (VON and RSAT) are specified within the function.

```
% BEGINNING OF FILE 'PMAX.m'
% Calculate voltage-limited dynamic Pout-fail
function PMAX_dBm = PMAX(VIMAX, RL, XL, VDC, IDC)

VON = 0.65; % V
RSAT = 15; % ohms
% Pmax_l = max power under linear (uncompressed) operation
Pmax_l = 0.5*RL*((VIMAX - VBIAS)/abs(RL+j*XL))^2;
ZL = RL + j*XL;
t = [1e-12:1e-12:220e-12];
f = 9.5e9;
w = 2*pi*f;
IP = sqrt(2*Pmax_l/real(ZL));
ii = IP*cos(w*t) + IDC;
vi = VDC - abs(ZL)*IP*cos(w*t + angle(ZL)); % raw waveform -- no compression

figure(1) % plot uncompressed dynamic waveform
plot(vi,ii)
hold on;

% calculate knee voltage at the I corresponding to minimum dynamic V
IP_VMIN = (VDC - VON - IBIAS*RSAT)/(abs(ZL)+RSAT)
VMIN = (IP_VMIN + IBIAS)*RSAT + VON
VKNEE = (RSAT*(VDC + abs(ZL)*IBIAS)+ abs(ZL)*VON)/(RSAT + abs(ZL))
VDC2 = VDC;
if min(vi) < VMIN
% minimum dynamic voltage swings below VKNEE --> compressed operation
     VDC2 = (VIMAX + VMIN)/2
end
% modified voltage waveform accounting for compression
```

```
vi_c = VDC2 - abs(ZL)*IP*cos(w*t + angle(ZL));

figure(1) % plot compressed dynamic waveform
plot(vi_c,ii)

Pmax = 0.5*RL*((VIMAX - VDC2)/abs(RL+j*XL))^2;
PMAX_dBm = 10*log10(1000*Pmax);

% END OF FILE 'PMAX.m'
```

A.2 Common-Base Volterra Series Analysis

Given the first-, second-, and third-order nonlinearity coefficients for a single bias point (I_C or V_{BE}, V_{CB}), the Matlab files presented here apply Volterra series to solve the first-order (h1calc.m), second-order (h2calc.m), and third-order (CB_Volterra.m) transfer functions using the y-matrix for a common-base SiGe HBT (ycalc.m). Ultimately, these functions calculate and return a value for IIP3 (in dBm) for the SiGe HBT in the common-base configuration at the bias point of interest. The two frequency tones are specified as f1 and f2, with f3 equal to either -f1 or -f2 (depending on whether the upper or lower intermodulation product is being examined). The external source and load impedances (Rsource and Rload, respectively) may be specified as either real or complex values. In practice, the nonlinearity coefficients should reside in a table spanning a range of bias, and thus the function CB_Volterra may be called in a loop to determine CB IIP3 across bias.

```
% BEGINNING OF FILE 'CB_Volterra.m'
% Two tone input common-base Volterra series analysis
function IIP3 = CB_Volterra(beta, gm, Cbe, Cbc, K2gm, K2Cbe, K2Cbc, K3gm, K3Cbe,
K3Cbc)

Rsource= 50;
Rload = 50;
f1 = 9.5E9; % fundamental at 9.5 GHz
f2 = 9.501E9; % 1 MHz tone spacing
f3 = -9.500E9;
gbe = gm/beta;
K2gbe = K2gm/beta;
K3gbe = K3gm/beta;

% H1 matrix calculations
H1f1 = h1calc(Rsource,Cbe,Cbc,Rload,gm,gbe,f1);
H1f2 = h1calc(Rsource,Cbe,Cbc,Rload,gm,gbe,f1);
H1f3 = h1calc(Rsource,Cbe,Cbc,Rload,gm,gbe,f1);
```

```
% H2 matrix calculations
H2f1f2 = h2calc(Rsource,Cbe,Cbc,Rload,gm,gbe,f1,f2,K2gbe,K2gm,K2Cbe,K2Cbc);
   % H2 matrix for f1,f2
H2f2f3 = h2calc(Rsource,Cbe,Cbc,Rload,gm,gbe,f2,f3,K2gbe,K2gm,K2Cbe,K2Cbc);
   % H2 matrix for f2,f3
H2f1f3 = h2calc(Rsource,Cbe,Cbc,Rload,gm,gbe,f1,f3,K2gbe,K2gm,K2Cbe,K2Cbc);
   % H2 matrix for f1,f3

% H3 calculations performed here
inl3gm = K3gm*H1f1(1)*H1f2(1)*H1f3(1) + (.66)*K2gm*(H1f1(1)*H2f2f3(1) +
         H1f2(1)*H2f1f3(1) + H1f3(1)*H2f1f2(1));
inl3gbe = K3gbe*H1f1(1)*H1f2(1)*H1f3(1) + (.66)*K2gbe*(H1f1(1)*H2f2f3(1) +
         H1f2(1)*H2f1f3(1) + H1f3(1)*H2f1f2(1));
inl3Cbe = -2*pi*j*(f1+f2+f3)*K3Cbe*H1f1(1)*H1f2(1)*H1f3(1) +
         (0.66)*2*pi*j*(f1+f2+f3)*K2Cbe*[H1f1(1)*H2f2f3(1) +
         H1f2(1)*H2f1f3(1) + H1f3(1)*H2f1f2(1)];
inl3Cbc = -2*pi*j*(f1+f2+f3)*K3Cbc*H1f1(2)*H1f2(2)*H1f3(2) +
         (0.66)*2*pi*j*(f1+f2+f3)*K2Cbc*[H1f1(2)*H2f2f3(2) +
         H1f2(2)*H2f1f3(2) + H1f3(2)*H2f1f2(2)];
Y3 = ycalc(Rsource,Cbe,Cbc,Rload,(f1+f2+f3),gm,gbe);
H3 = inv(Y3)*[-inl3Cbe-inl3gbe-inl3gm;inl3Cbc-inl3gm];

IIP_num = (H1f1(2));
IIP_denom = 6*Rsource*(H3(2));
IIPfull = abs(IIP_num/IIP_denom);
IIP3 = 10*log10(1000*IIPfull);

% END OF FILE 'CB_Volterra.m'


% BEGINNING OF FILE 'h1calc.m'
% H1 calculating function for CB mode
function Hfinal = h1calc(Rsource, Cbe, Cbc, Rload, gm, gbe, f1)

Y = ycalc(Rsource,Cbe,Cbc,Rload,f1,gm,gbe);
Ys = 1/(Rsource);
Hfinal = inv(Y)*[Ysource;0];

% END OF FILE 'h1calc.m'


% BEGINNING OF FILE 'h2calc.m'
% H2 calculating function for CB mode
function Hfinal2 = h2calc(Rsource, Cbe, Cbc, Rload, gm, gbe, f1, f2, K2gbe, K2gm,
K2Cbe, K2Cbc)

H1f1 = h1calc(Rsource,Cbe,Cbc,Rload,gm,gbe,f1);
H1f2 = h1calc(Rsource,Cbe,Cbc,Rload,gm,gbe,f2);
```

```
inl2gbe = K2gbe*H1f1(1)*H1f2(1); % 2nd order nonlinearity due to gbe
inl2gm = K2gm*H1f1(1)*H1f2(1); % 2nd order nonlinearity due to gm
inl2Cbe = K2Cbe*j*2*pi*(f1+f2)*H1f1(1)*H1f2(1); % 2nd order nonlinearity due
to Cbe
inl2Cbc = K2Cbc*j*2*pi*(f1+f2)*H1f1(2)*H1f2(2); % 2nd order nonlinearity due
to Cbc
Y = ycalc(Rsource,Cbe,Cbc,Rload,(f1+f2),gm,gbe);

Hfinal2 = inv(Y)*[-inl2gbe-inl2gm-inl2Cbe;inl2Cbc-inl2gm];

% END OF FILE 'h2calc.m'


% BEGINNING OF FILE 'ycalc.m'
% Admittance matrix calculator for CB mode
function Yfinal = ycalc(Rsource, Cbe, Cbc, Rload, f1, gm, gbe)

Ys = 1/(Rsource);
Yl = 1/(Rload);
A = j*2*pi*Cbe*f1;
B = j*2*pi*Cbc*f1;

Yfinal = [Ys+gbe+gm+A 0;gm -(B+Yl)];

% END OF FILE 'ycalc.m'
```

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